

SF1

Rev: 1.0


Revision History :

1. Ver A: Initial L4S6MG
2. Ver B:
 - I. P12 Del Pull-down when no 1394
 - II. P14 Modify clock gen enable & bus select CKT
 - III. P20 Modify PCI3 routing to DABC & Del AC97 reset CKT
 - IV. P21 Add D30 for EZJ1-CDROM
 - V. P22 Modify UD2+-, UD3+- NET
 - VI. P25 Add COM2 CP8, CP9
 - VII. P26 Modify FAN CTRL BJT for 772 to 2907
 - VIII. P28 Modify FPMIC NET
 - IX. P29 Modify VCCBUS CKT & Del CMF4, RN15
 - X. P30 RTL8100C/8110S Co-layout
 - XI. P31 Modify VCC3_DUAL, SB_M, SB1.8V, AUX_IVDD CKT
 - XII. P32 Modify VCC1.8V, VDDQ, IVDD, DDRVTT CKT
 - XIII. P33 ADP3180/RT9247 Co-layout
 - XIV. P34 Add LJ2, LSMI1 & Modify EZJ1-CDROM & Modify BATOK CKT
3. Ver C:
 - I. Del EZJ1(P11, P21, P34)
 - II. Del FANCTL#2, WOL1 and Modify HW temp monitor for TF(P23, P26)
 - III. Add Jack-detect circuit(P27, P28)
 - IV. Del CNR1(P20)
 - V. Del RN18(P14)
 - VI. Modify VCC_DUAL circuit For S5(P31)
 - VII. Add SR for 661FX and R371 for DDRVTT(P32)
 - VIII. Add LAN RCR circuit(P30)
 - IX. meet 648/661/660 new 3in1 trace length
4. Ver 1.0:
 - I. Add LMDN1 & Modify for ALC202A&655(P27)
 - II. USB+LUSB(P22)
 - III. Add CPU Temp header(P04)
 - IV. VGA1/COM3 co-layout(P25)
 - V. Add WOL1, WOM1 and FAN_CTRL2(P26)
 - VI. Modify IR header(P24)
 - VII. Modify VRD for 9.0 + 10.0(P33)

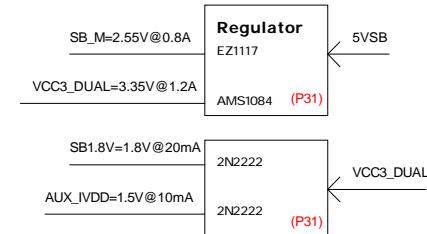
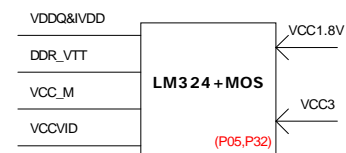
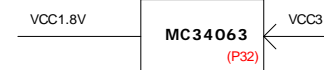
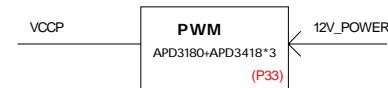
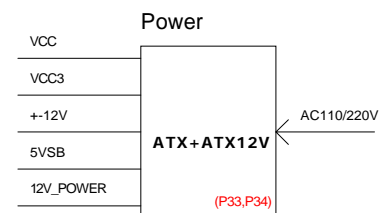
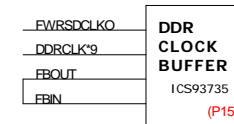
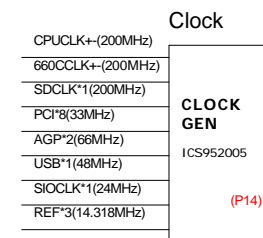
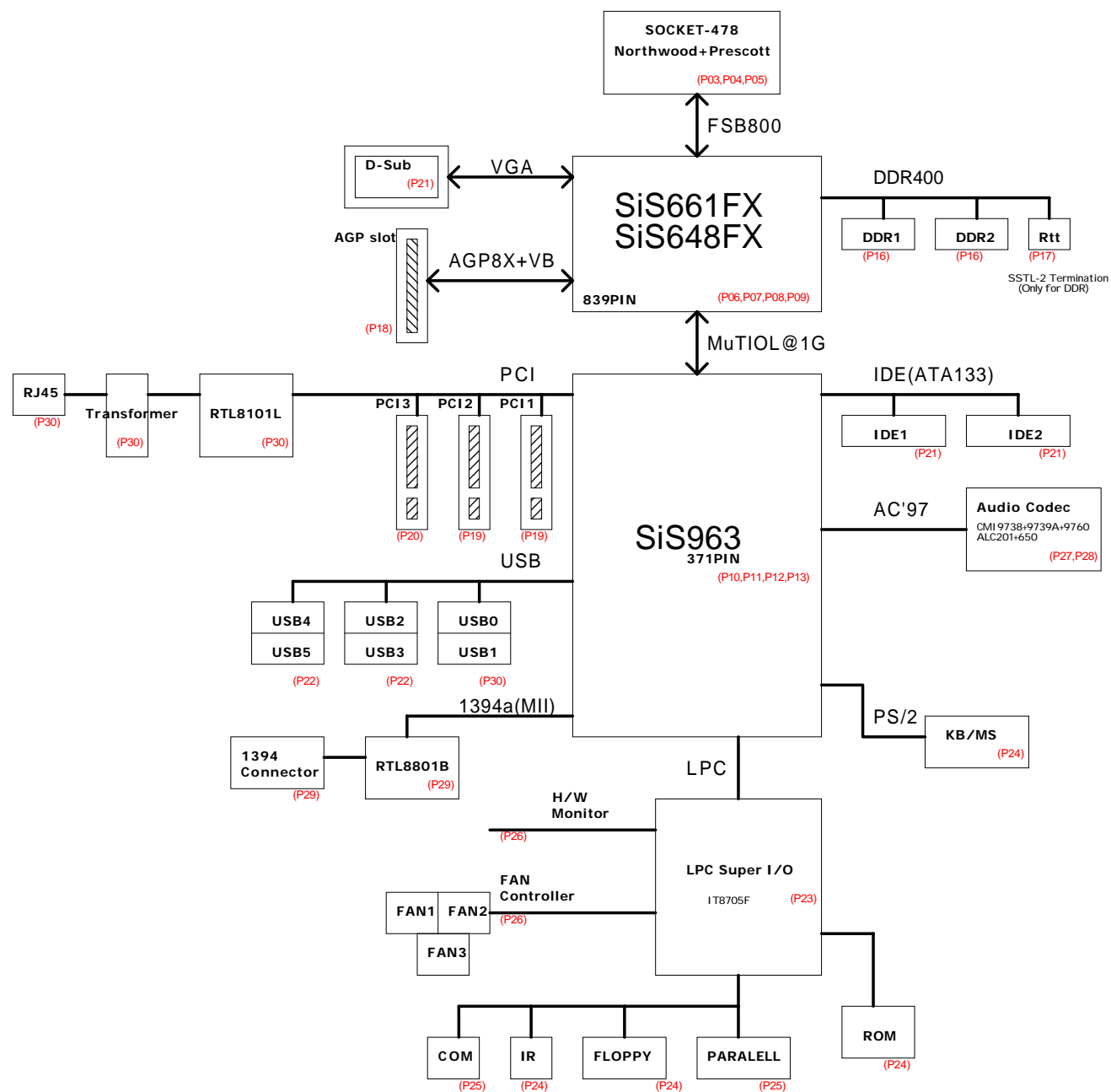
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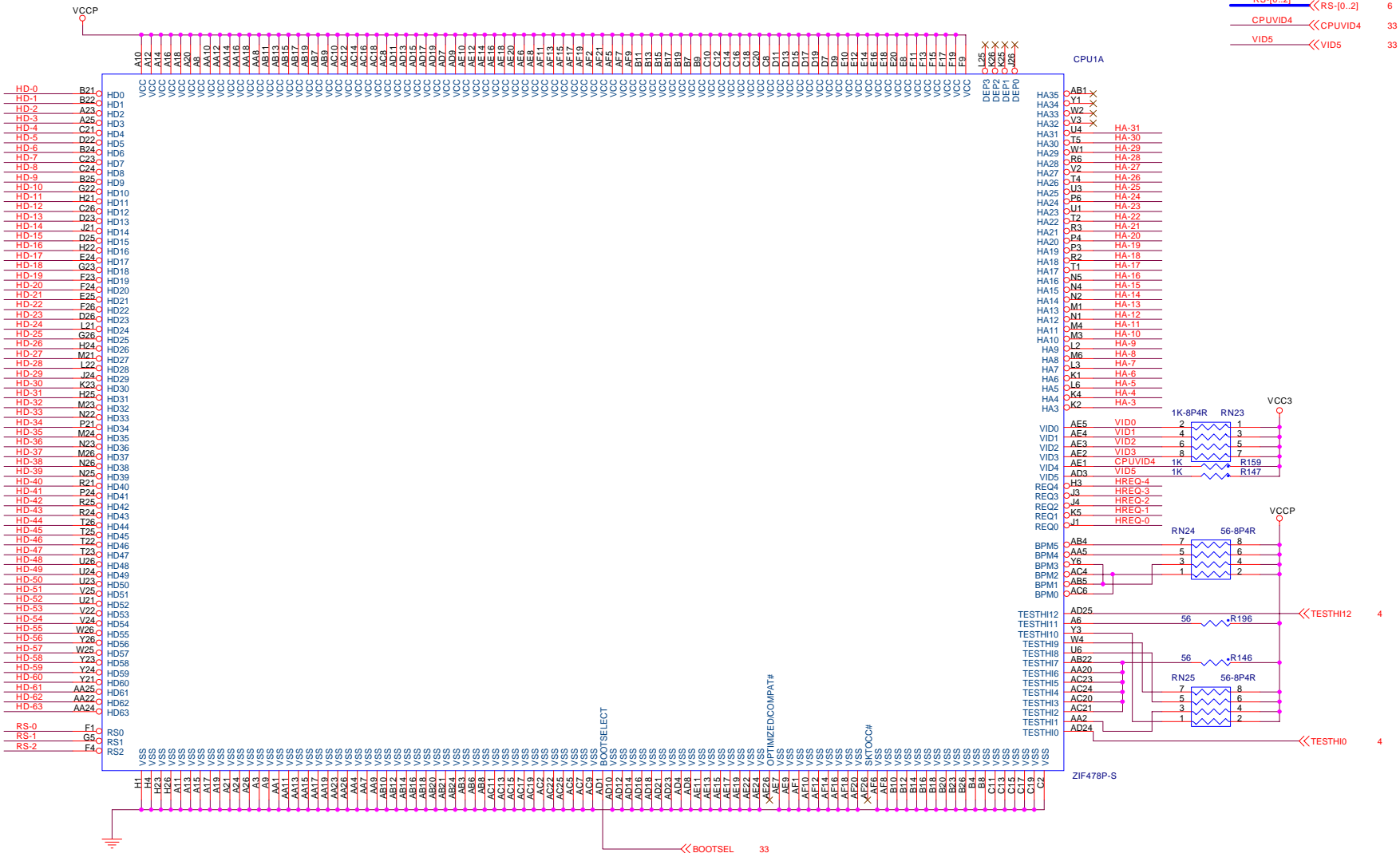
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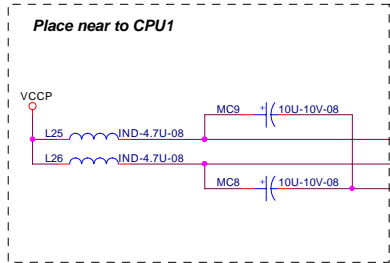
01. Cover Sheet
02. Block Diagram
03. Socket478-1
04. Socket478-2
05. Decoupling Circuit
06. SiS648FX-1 (HOST / AGP)
07. SiS648FX-2 (Memory)
08. SiS648FX-3 (HyperZip)
09. SiS648FX-4 (Power)
10. SiS963-1 (PCI / IDE / HyperZip)
11. SiS963-2 (Misc. Signals)
12. SiS963-3 (USB)
13. SiS963-4 (Power)
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15. Clock Buffer
16. DIMM 1, 2
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22. USB Connector
23. ITE8705
24. KB/MS/ROM/FDC/IR
25. COM 1,2 / LPT
26. HM/FAN/RING/LPC
27. Audio Codec
28. Audio Interface
29. IEEE1394 (RTL8801B)
30. LAN RTL8100C/8110S
31. DUAL 5V, 3V& SB Regulator
32. Voltage Regulator
33. Vcore Power
34. ATX/Panel/RTC

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System Block Diagram





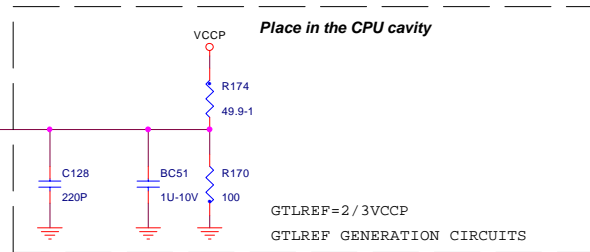


Strobe signals與旁邊trace保持21mils距離

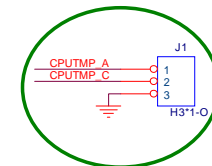
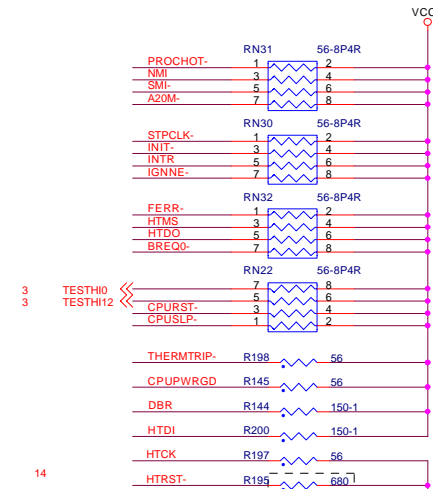
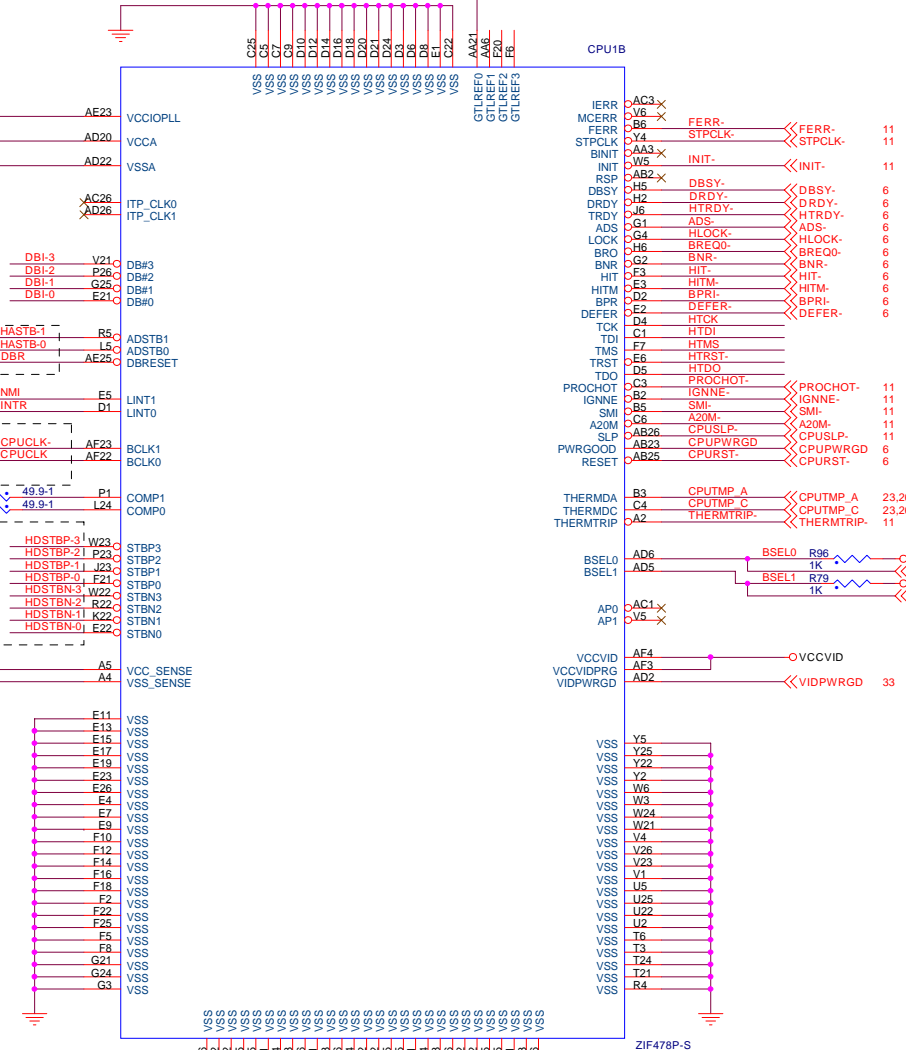
**Differential Clock signals
成 離暖妮娃u,
並與旁邊trace保持18mils Z離**

**Differential Strobe signals
成 離暖妮娃u,
並與旁邊trace保持21mils Z離**

	R175, R183
COMPATIBLE	49.9_1%
OPTIMIZED	61.9_1%

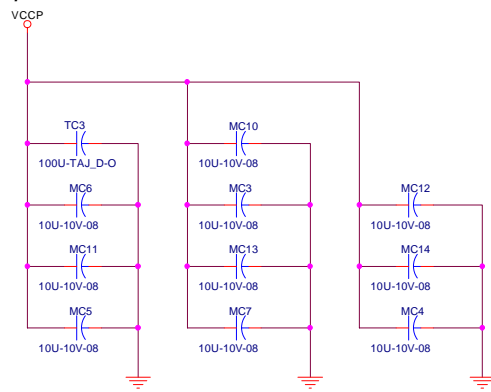


DBI-[0..3] << DBI-[0..3] 6
HDSTBN-[0..3] << HDSTBN-[0..3] 6
HDSTBP-[0..3] << HDSTBP-[0..3] 6
HASTB-[0..1] << HASTB-[0..1] 6

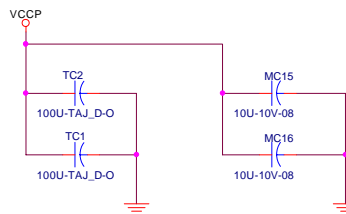


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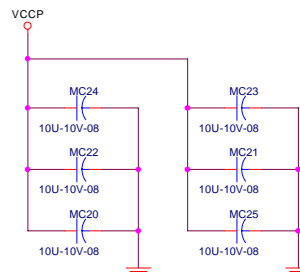
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

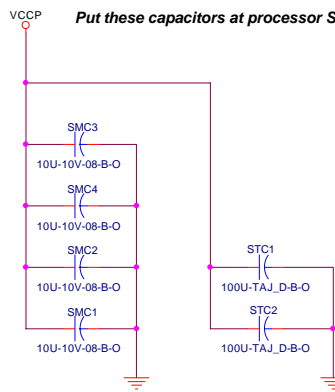


Put these capacitors at processor SOUTH SIDE

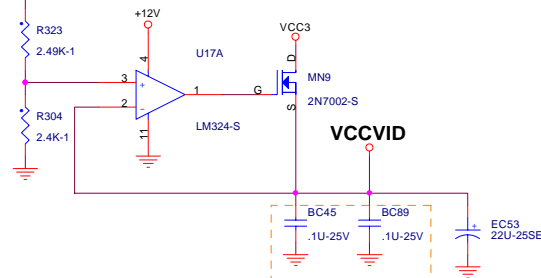


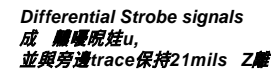
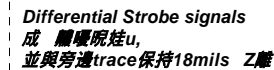
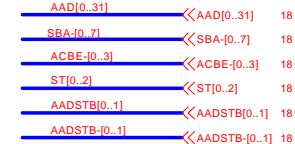
P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

Put these capacitors at processor SOLDER SIDE



2.5VREF





Title				SF1/648FX			
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Custom	<i>SiS660-1 (Host / AGP)</i>						1.0
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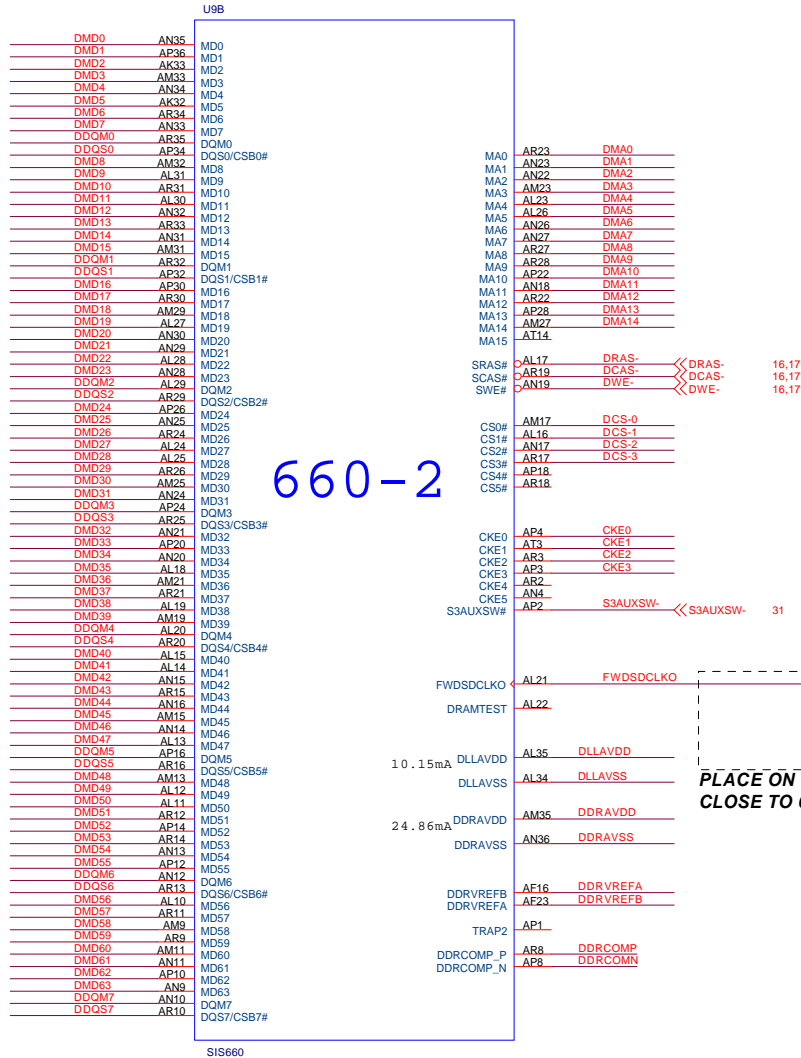
	R143	R133
648	20 1%	110 1%
648FX	14 1%	100 1%
661FX	14 1%	100 1%
661FXLV	14 1%	100 1%

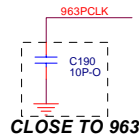
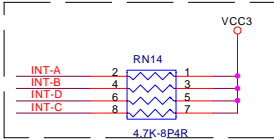
	HNCVREF pin B22
648	Voltage divider
648FX	NC
661FX	
661FXLV	

接在一起再接地

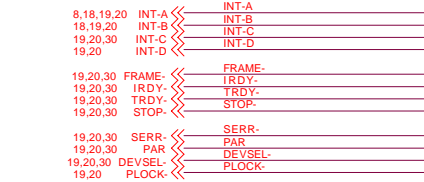
接在一起再接地

DMD[0..63]	<<DMD[0..63]	16,17
DDQM[0..7]	<<DDQM[0..7]	16,17
DDQS[0..7]	<<DDQS[0..7]	16,17
DMA[0..14]	<<DMA[0..14]	16,17
DCS-[0..3]	<<DCS-[0..3]	16,17
CKE[0..3]	<<CKE[0..3]	16

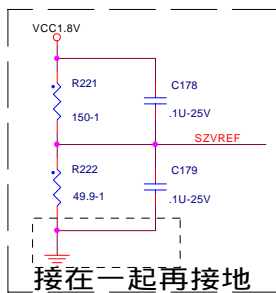




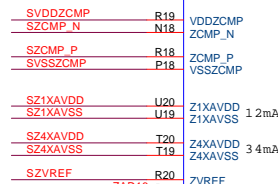
19,20,30 CBE-[0..3] << CBE-[0..3]



CLOSE TO 963



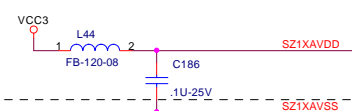
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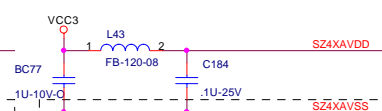
HyperZip

8 ZAD[0..16] << ZAD[0..16]

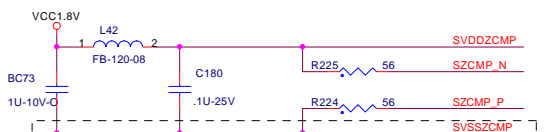
Analog Power supplies of Transip function for 96X Chip.



接在一起再接地



接在一起再接地



接在一起再接地

U11A

PCI

IDE

963-1

1.0mA IDEAVDD IDEAVSS

ICHRDYA

IDREQA

IDEIQA

CBLIDA

IIOR#A

IIOW#A

IDACK#A

IDSAA2

IDSAA1

IDSAA0

IDCSA1#

IDCSA0#

ICHRDYB

IDREQB

IDEIOB

CBLIDB

IIOR#B

IIOW#B

IDACK#B

IDSAB2

IDSAB1

IDSAB0

IDCSB1#

IDCSB0#

IDA0

IDA1

IDA2

IDA3

IDA4

IDA5

IDA6

IDA7

IDA8

IDA9

IDA10

IDA11

IDA12

IDA13

IDA14

IDA15

IDB0

IDB1

IDB2

IDB3

IDB4

IDB5

IDB6

IDB7

IDB8

IDB9

IDB10

IDB11

IDB12

IDB13

IDB14

IDB15

SIS963

VCC1.8V

C192

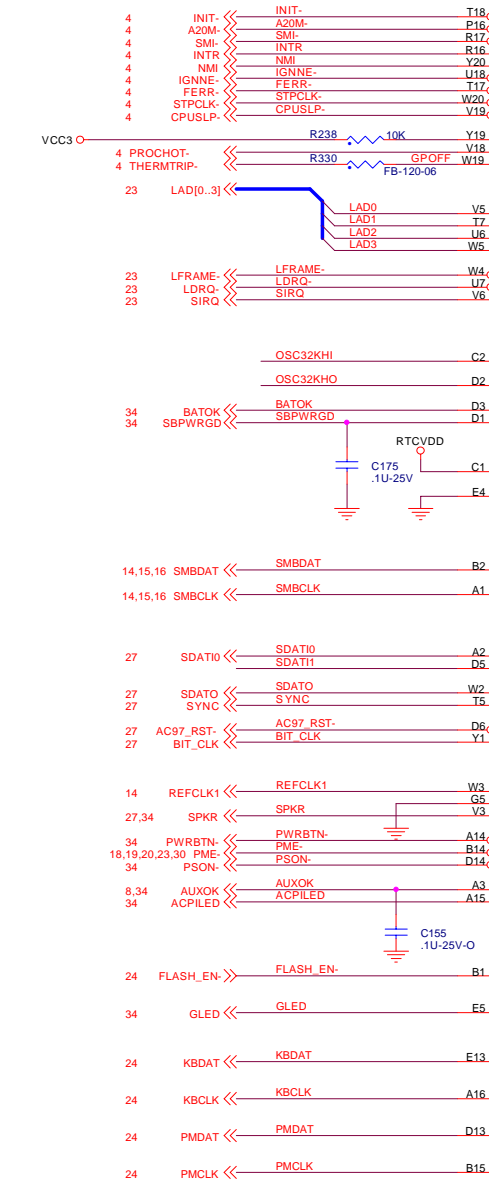
.1U-25V



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Programable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)



CPU_S

APIC

LPC

RTC

GPIO

AC97

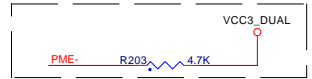
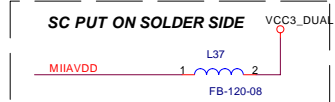
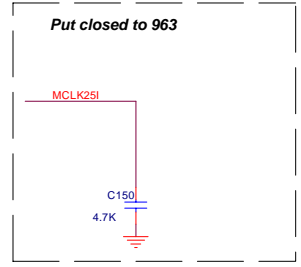
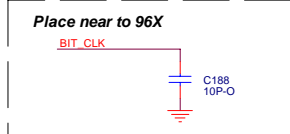
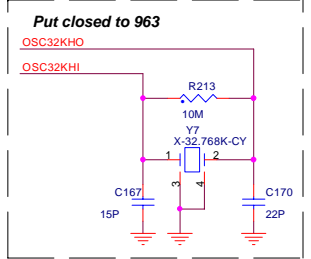
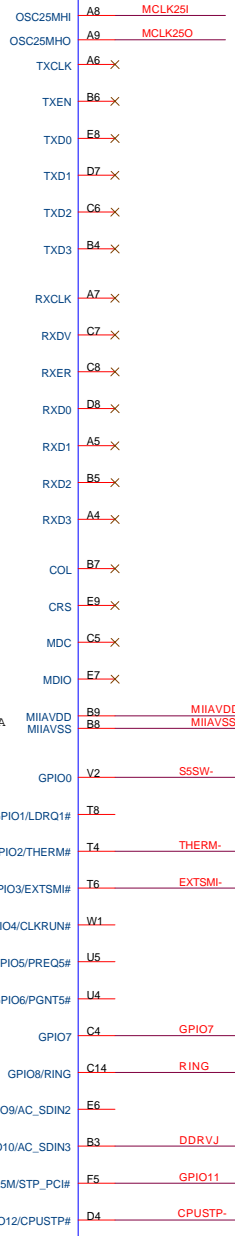
ACPI
/others

KBC
/geyserville

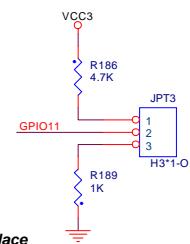
MII

GPIO

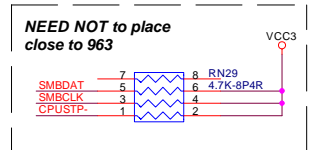
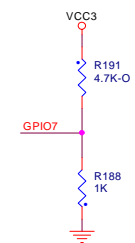
SIS963



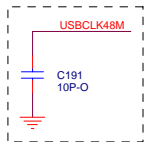
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close to 963



NEED NOT to place
close to 963

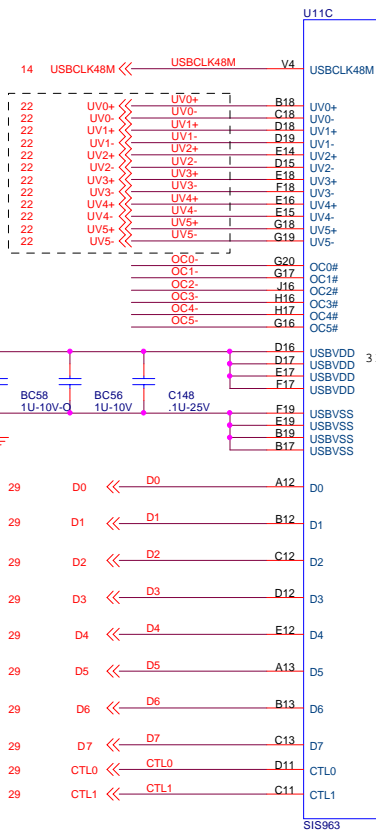


	0	1
GPIO7	W 1394PHY	W/O 1394PHY
GPIO11	W/O S3	W S3



CLOSE TO 963

Differential signals
成雙 雙端接u

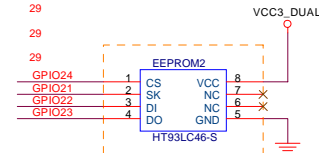
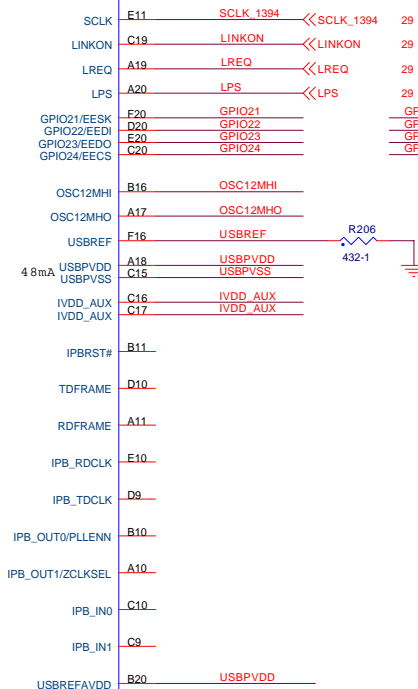
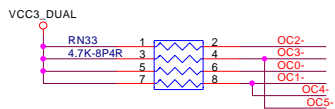


USB

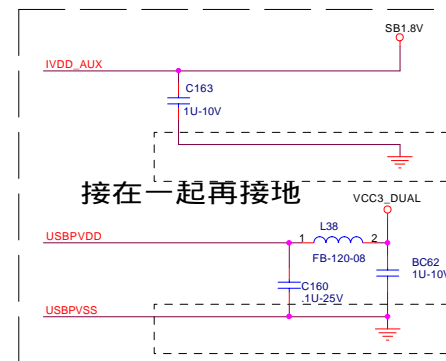
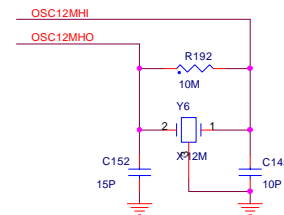
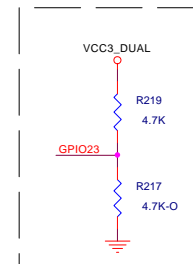
963-3

1394

SIS963



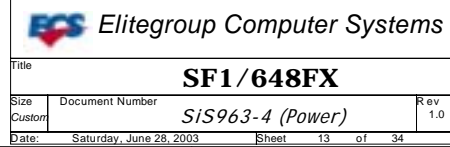
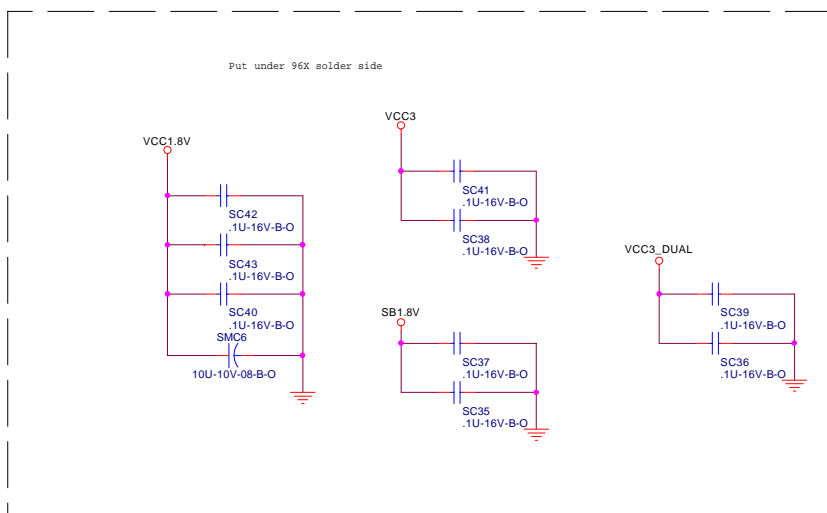
EEDO	High	Low
1394	Enable	Disable



接在一起再接地

接在一起再接地

	0	1	Default	
SPKR(LPC_addr mapping)	disable	enable	R169 un-stuff	yes
SYNC(PCICLK PLL)	enable	disable	NONE	yes
OC2-(SB_debug mode)	enable	disable	R171 un-stuff	NO
SDAT0(Trap from)	PCI AD	ROM	R170 stuff	yes



Main Clock Generator

Del C157

在CLK1底下鋪GND銅箔

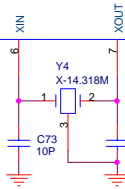
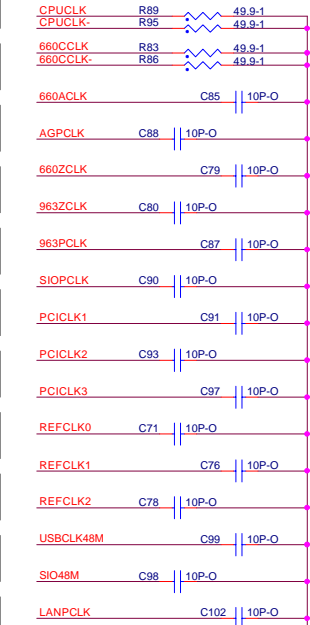
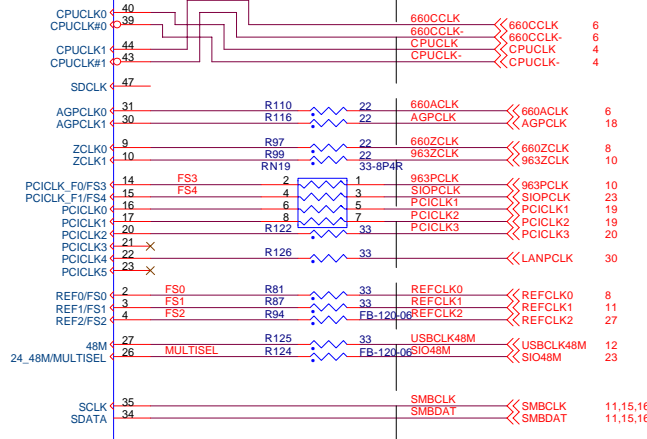
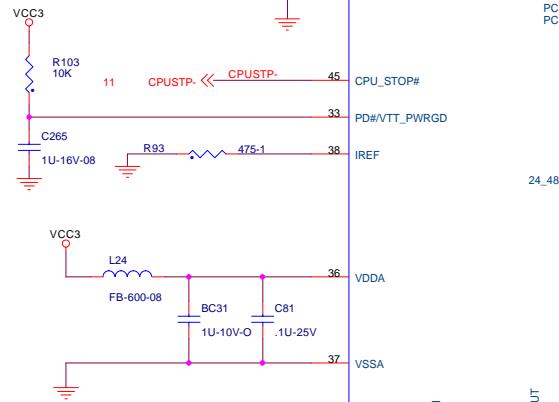
CLK1
ICS952005CF-S

PLACE TO EVERY POWER PIN

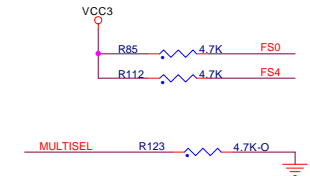
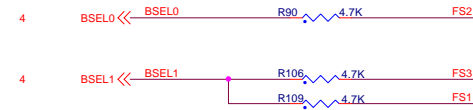
Damping Resistors
Place near to CLK1

By-Pass Capacitors

Place near to the Clock Outputs



Frequency Selection



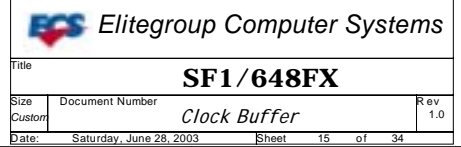
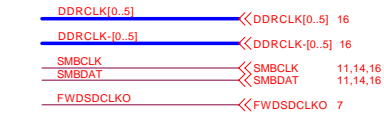
SIS660 CLOCK									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	AGPCLK (MHz)	PCICLK (MHz)	2CLK (MHz)
0	0	0	0	0	100.20	100.20	66.80	33.40	80.16
0	0	0	1	0	100.20	133.60	66.80	33.40	80.16
0	0	0	1	1	100.20	200.40	66.80	33.40	80.16
0	0	0	1	1	100.20	167.00	66.80	33.40	80.16
0	0	1	0	0	133.60	100.20	66.80	33.40	80.16
0	0	1	0	1	133.60	133.60	66.80	33.40	80.16
0	0	1	1	0	133.60	200.40	66.80	33.40	80.16
0	0	1	1	1	133.60	167.00	66.80	33.40	80.16
0	1	0	0	0	200.50	100.03	66.68	33.34	80.02
0	1	0	0	1	200.50	133.37	66.68	33.34	80.02
0	1	0	1	0	200.50	200.50	66.68	33.34	80.02
0	1	0	1	1	200.50	160.04	66.68	33.34	80.02
0	1	1	0	0	166.70	100.03	66.68	33.40	80.16
0	1	1	0	1	166.70	133.36	66.68	33.40	80.16
0	1	1	1	0	166.70	200.50	66.68	33.34	80.02
0	1	1	1	1	166.70	166.70	66.68	33.34	80.02

SIS660 CLOCK									
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	AGPCLK (MHz)	PCICLK (MHz)	2CLK (MHz)
1	0	0	0	0	100.20	100.20	66.80	33.40	133.60
1	0	0	1	0	100.20	133.60	66.80	33.40	133.60
1	0	0	1	1	100.20	200.40	66.80	33.40	133.60
1	0	0	1	1	100.20	167.00	66.80	33.40	133.60
1	0	1	0	0	133.60	100.20	66.80	33.40	133.60
1	0	1	0	1	133.60	133.60	66.80	33.40	133.60
1	0	1	1	0	133.60	200.40	66.80	33.40	133.60
1	0	1	1	1	133.60	167.00	66.80	33.40	133.60
1	1	0	0	0	200.50	100.03	66.68	33.34	133.37
1	1	0	0	1	200.50	133.37	66.68	33.34	133.37
1	1	0	1	0	200.50	200.50	66.68	33.34	133.37
1	1	0	1	1	200.50	160.04	66.68	33.34	133.37
1	1	1	0	0	166.70	100.03	66.68	33.40	133.60
1	1	1	0	1	166.70	133.36	66.68	33.40	133.60
1	1	1	1	0	166.70	200.50	66.68	33.34	133.37
1	1	1	1	1	166.70	166.70	66.68	33.34	133.37

CPU=100 (BSEL=00), FS=10001-->100/133/133
CPU=133 (BSEL=01), FS=10101-->133/133/133
CPU=166 (BSEL=11), FS=11111-->166/166/133
CPU=200 (BSEL=10), FS=11011-->200/160/133

Clock Buffer (DDR)

By-Pass Capacitors
Place near to the Clock Buffer



NOTE:

VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

7,17
7,17
7,17

DRAS-
DCAS-
DWE-

DRAS- 154 RAS#
DCAS- 65 CAS#
DWE- 63 WE#

DCS-0 157 S0#
DCS-1 158 S1#
X 71 NC(S2#)
X 163 NC(S3#)

CKE0 21 CKE0
CKE1 111 CKE1

DDRCLK1 137 CK0
DDRCLK0 16 CK1
DDRCLK2 76 CK2
DDRCLK-1 138 CK0#
DDRCLK-0 17 CK1#
DDRCLK-2 75 CK2#

addr =
1010000b

DDR-BL

VCC_DIMM

NOTE:

VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

7,17
7,17
7,17

DRAS-
DCAS-
DWE-

DRAS- 154 RAS#
DCAS- 65 CAS#
DWE- 63 WE#

DCS-2 157 S0#
DCS-3 158 S1#
X 71 NC(S2#)
X 163 NC(S3#)

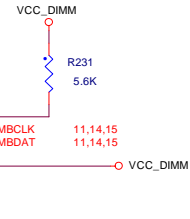
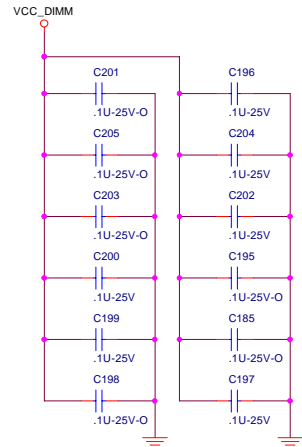
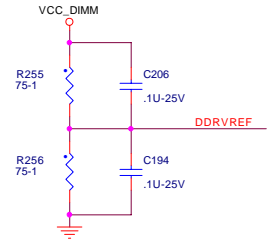
CKE2 21 CKE0
CKE3 111 CKE1

DDRCLK4 137 CK0
DDRCLK3 16 CK1
DDRCLK3 76 CK2
DDRCLK-4 138 CK0#
DDRCLK-3 17 CK1#
DDRCLK-5 75 CK2#

addr =
1010001b

DDR-BL

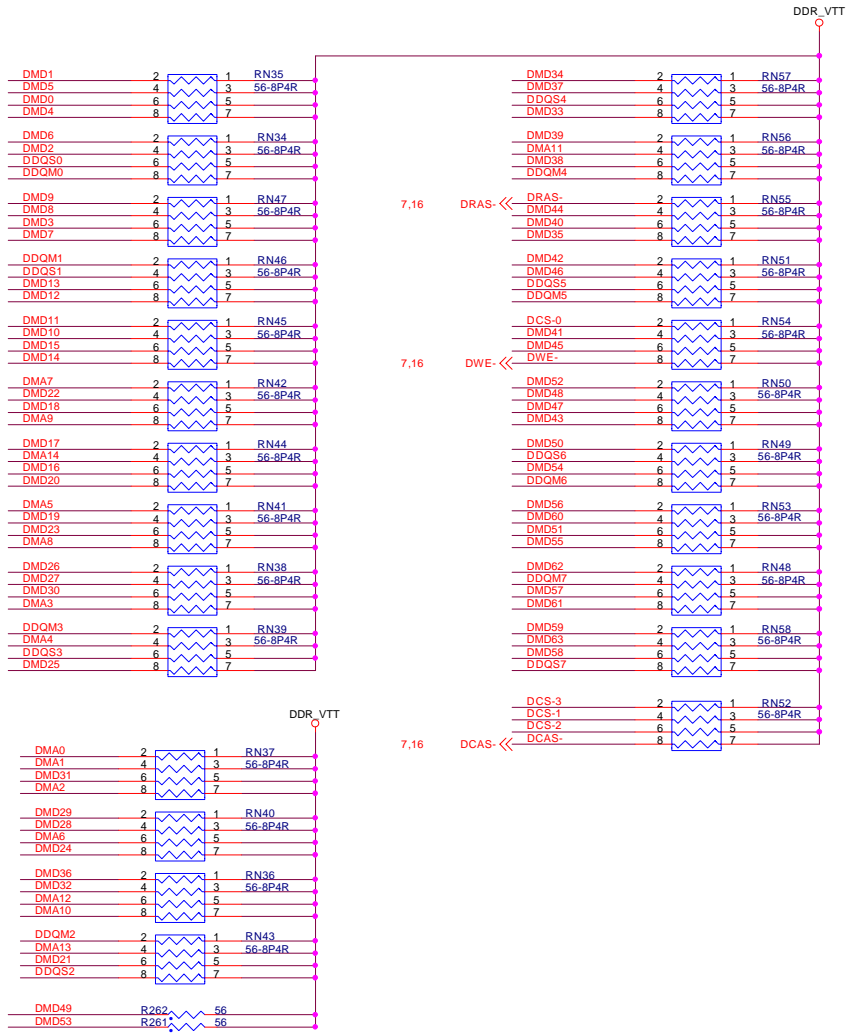
DMD[0..63] << DMD[0..63] 7,17
DMA[0..14] << DMA[0..14] 7,17
DDQM[0..7] << DDQM[0..7] 7,17
DDQS[0..7] << DDQS[0..7] 7,17
DCS[0..3] << DCS[0..3] 7,17
CKE[0..3] << CKE[0..3] 7
DDRCLK[0..5] << DDRCLK[0..5] 15
DDRCLK-[0..5] << DDRCLK-[0..5] 15



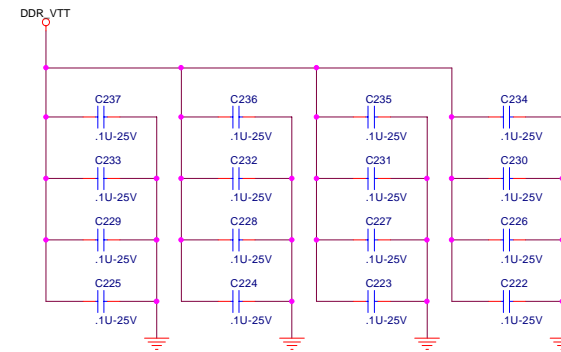
SSTL-2 Termination Resistors

	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	1.0	33
MA/Control	LV-CMOS	1.0	SSTL-2	1.0	33
CS	LV-CMOS	0	SSTL-2	1.0	33
EKE	0.3V		2.5V		47

DMD[0..63]	<<DMD[0..63]	7,16
DMA[0..14]	<<DMA[0..14]	7,16
DDQM[0..7]	<<DDQM[0..7]	7,16
DDQS[0..7]	<<DDQS[0..7]	7,16
DCS-[0..3]	<<DCS-[0..3]	7,16

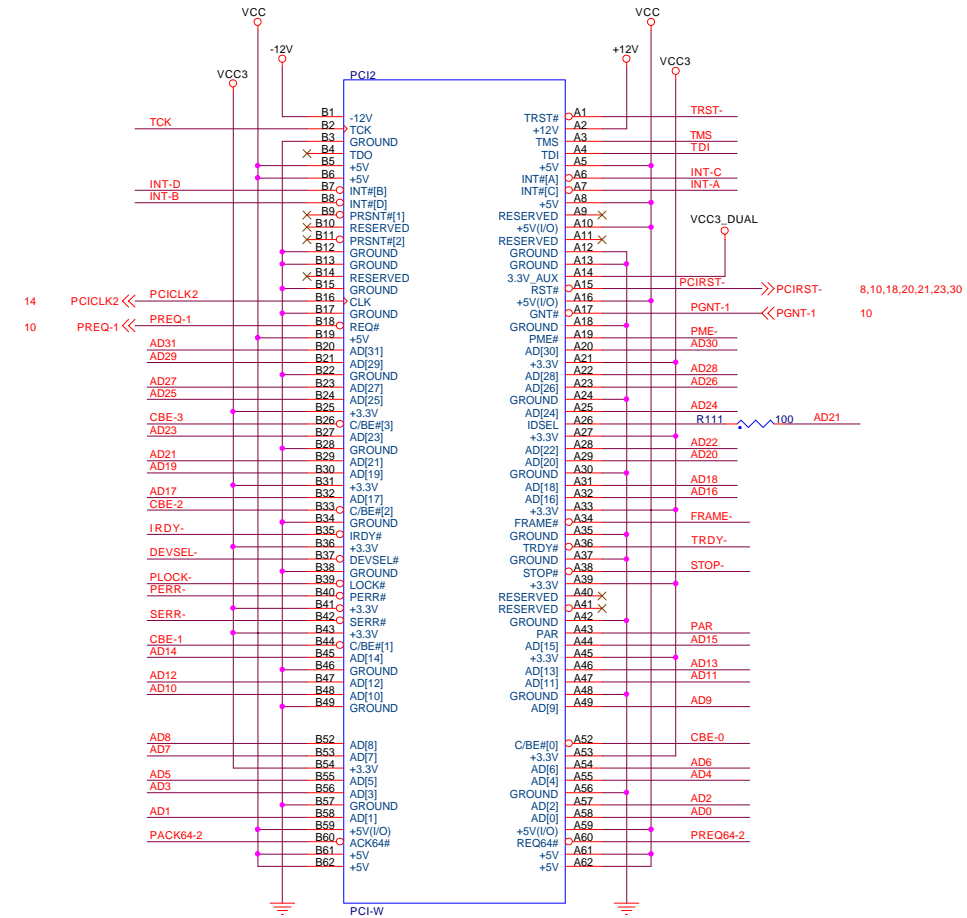
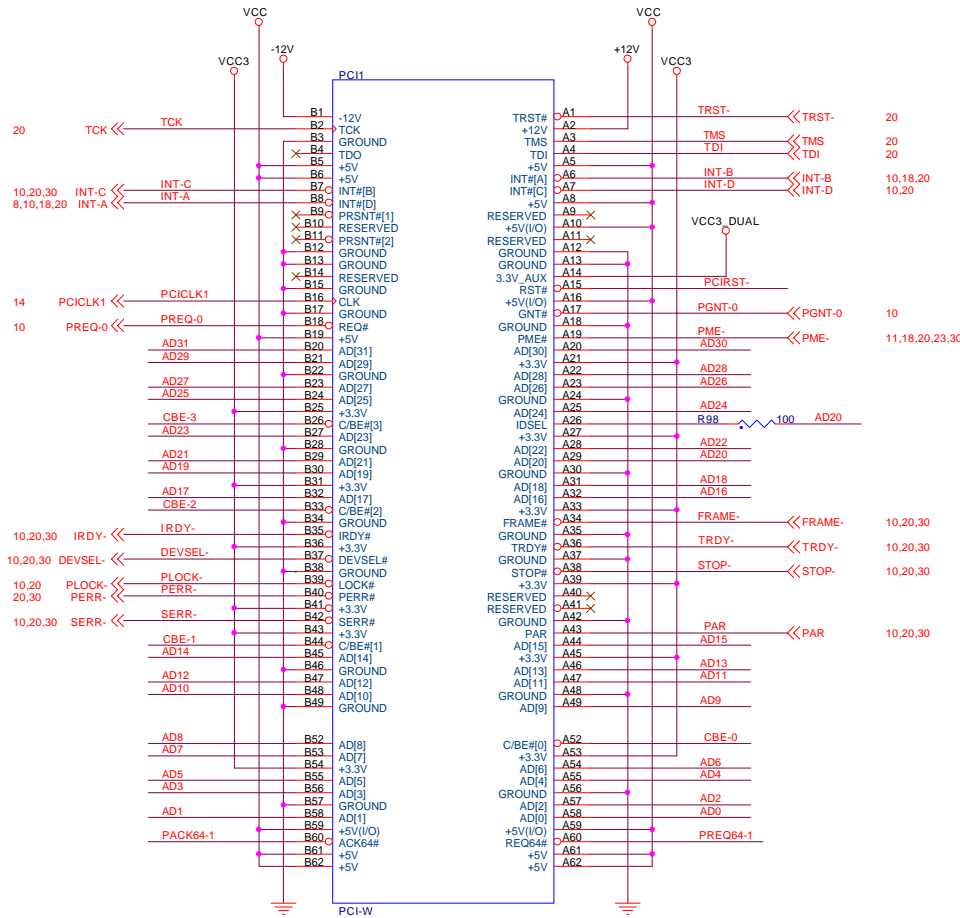


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND 0603 Package placed within 200mils of VTT Termination R-packs



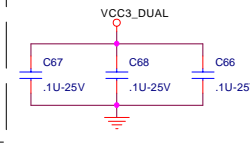
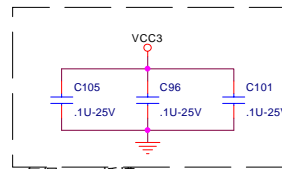
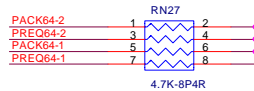
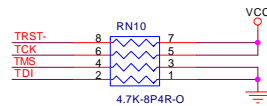
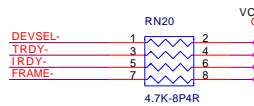
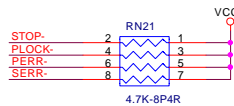
PCI Slot 1 & 2

10,20,30 CBE-[0..3] << CBE-[0..3]
10,20,30 AD[0..31] << AD[0..31]

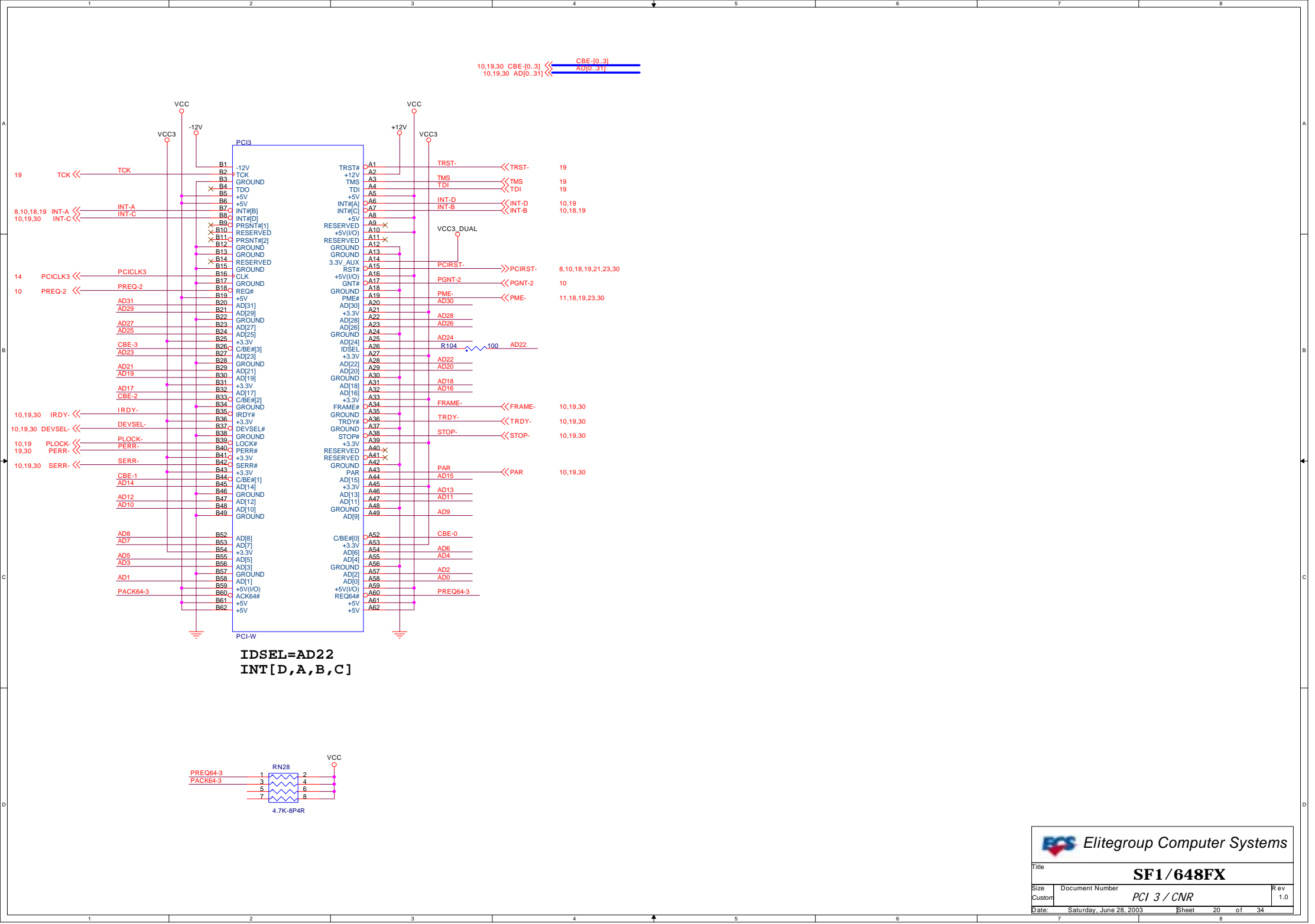


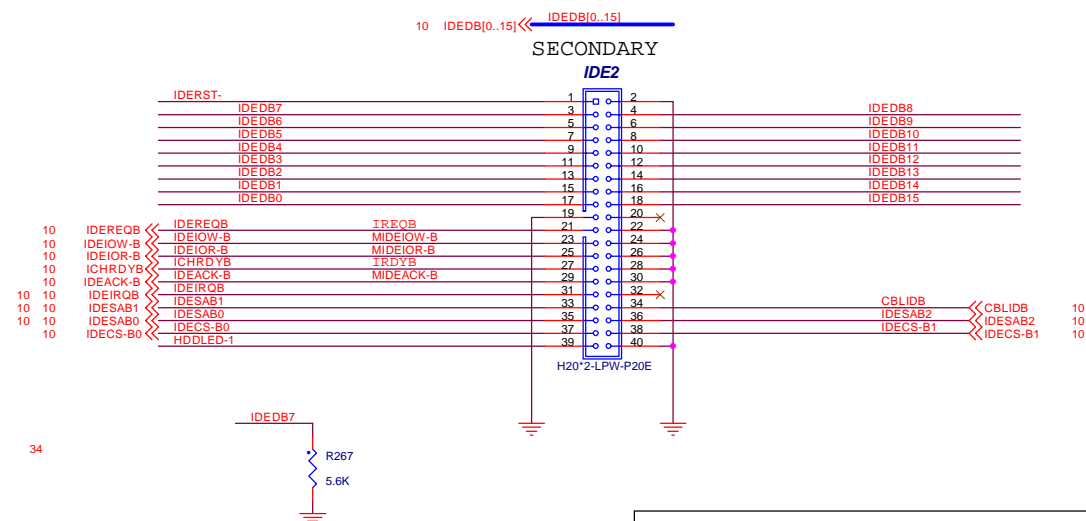
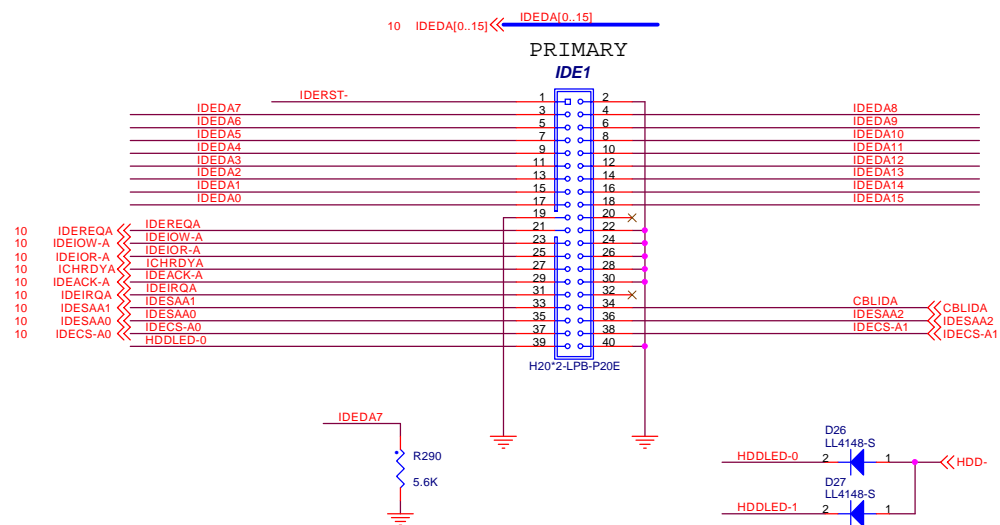
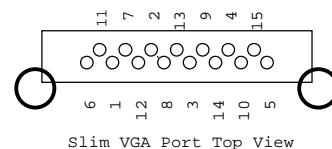
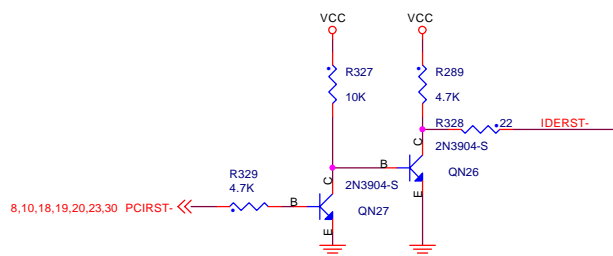
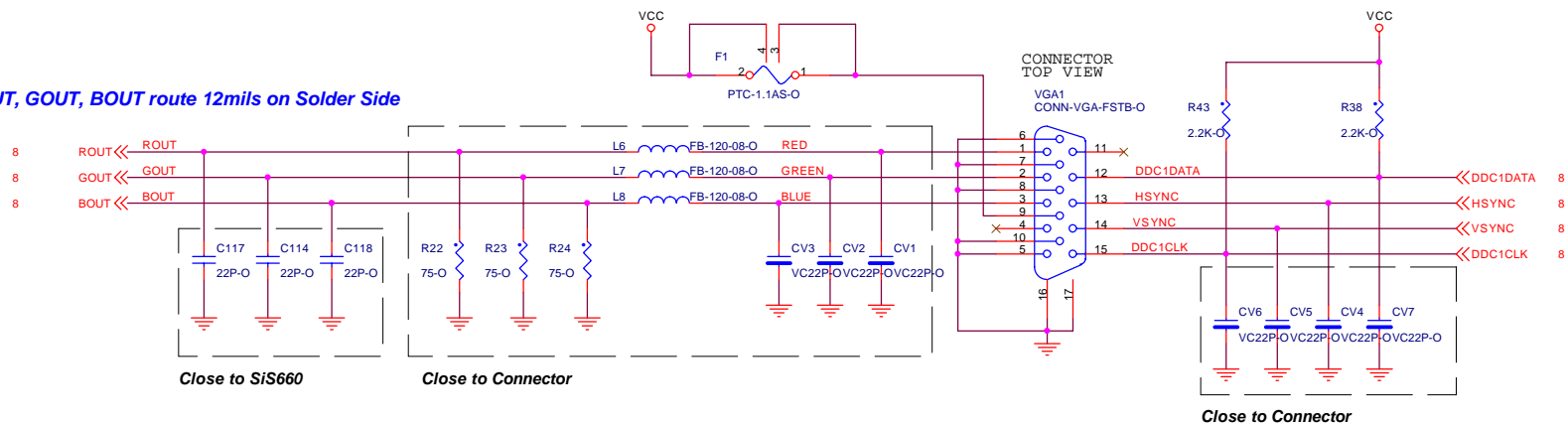
IDSEL=AD20
INT[B,C,D,A]

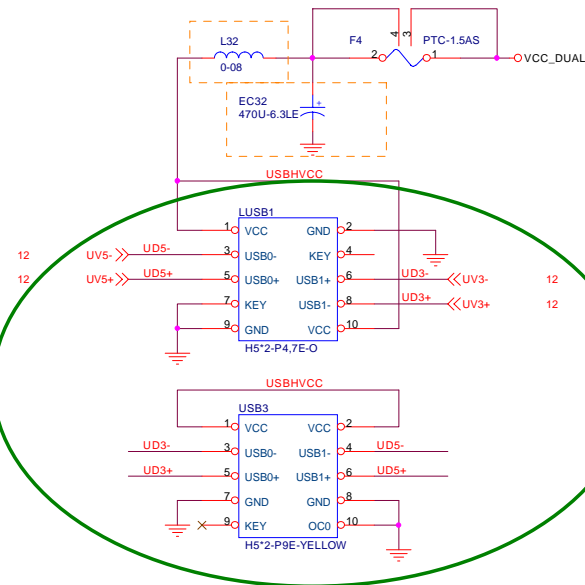
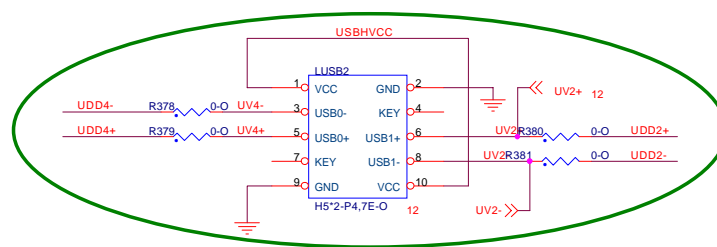
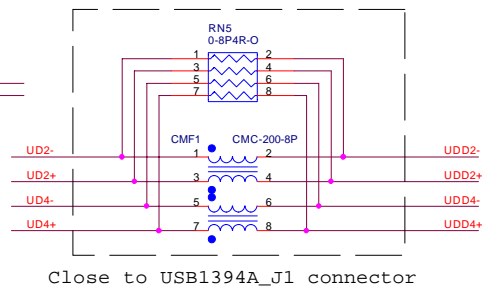
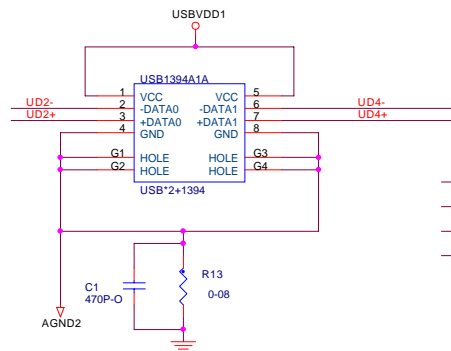
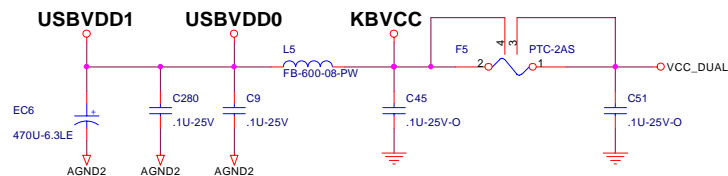
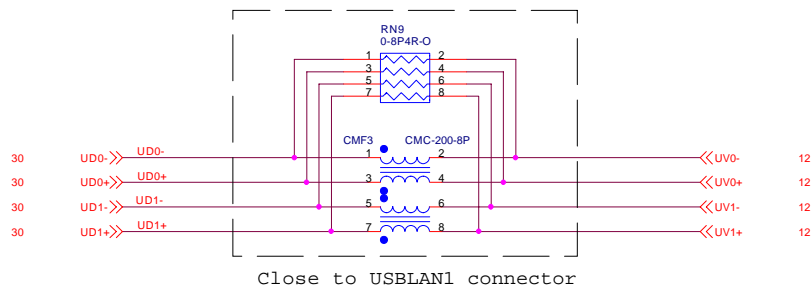
IDSEL=AD21
INT[C,D,A,B]

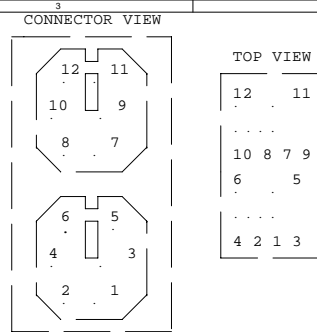


每個 PCI 插槽 pin A33
各放一顆

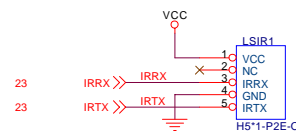
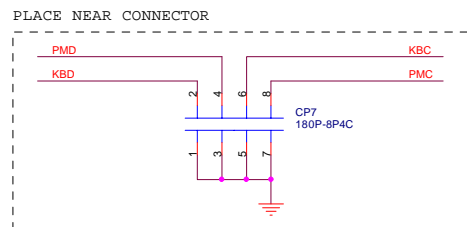
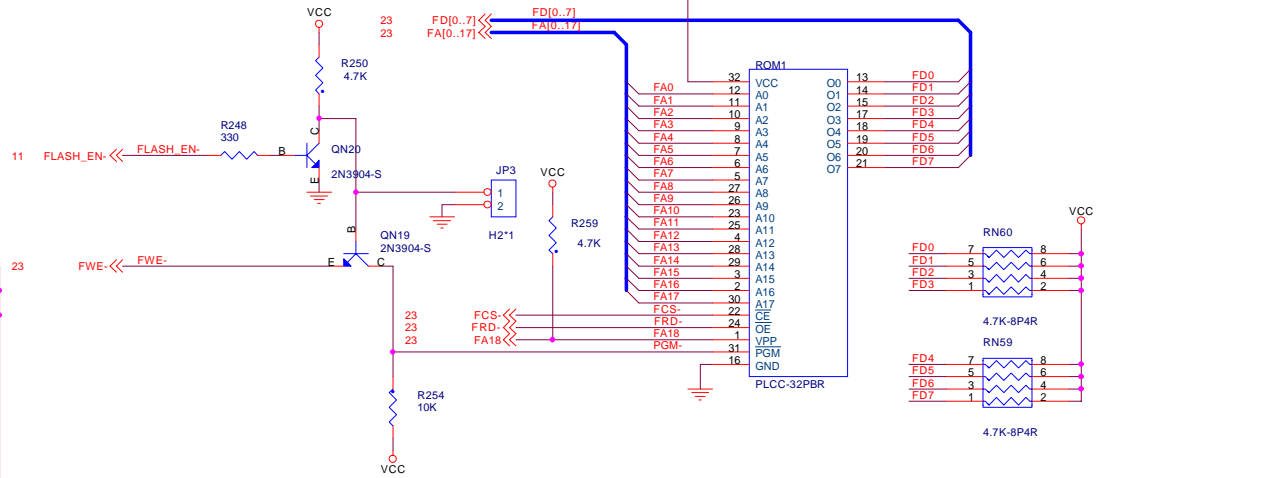
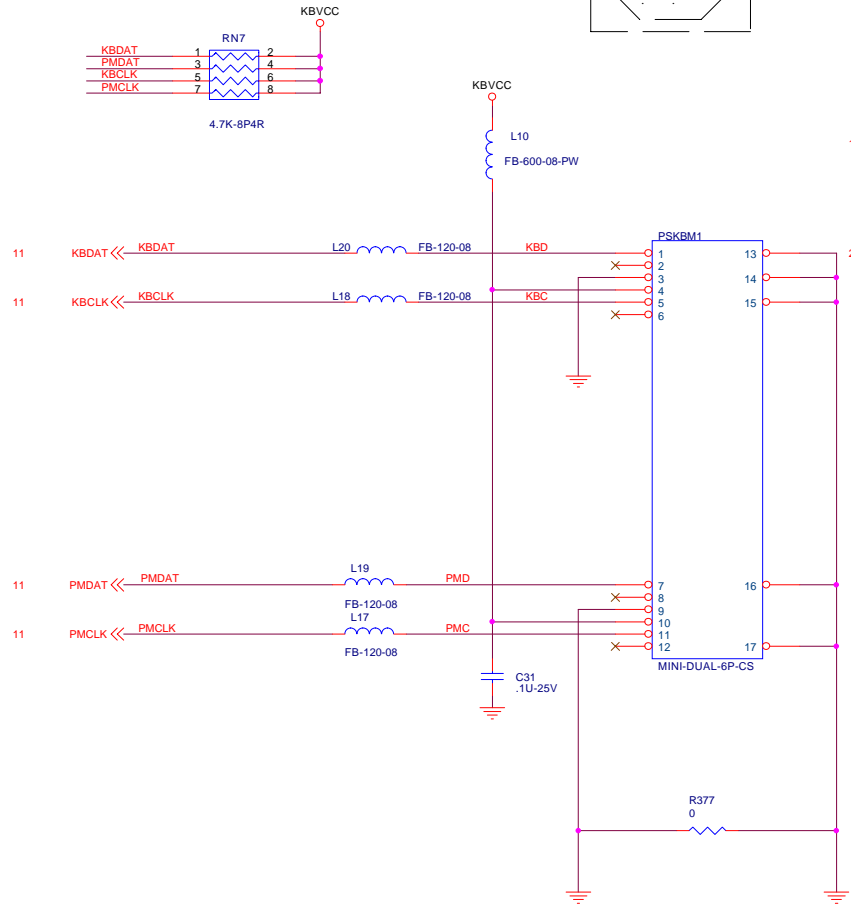








JP3	BIOS PROTECT
OPEN	DISABLE
SHORT	ENABLE

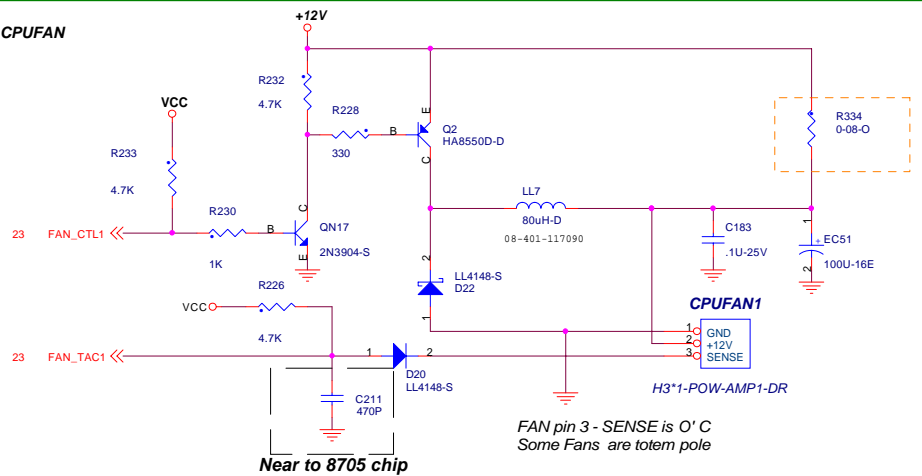


IR CONNECTOR

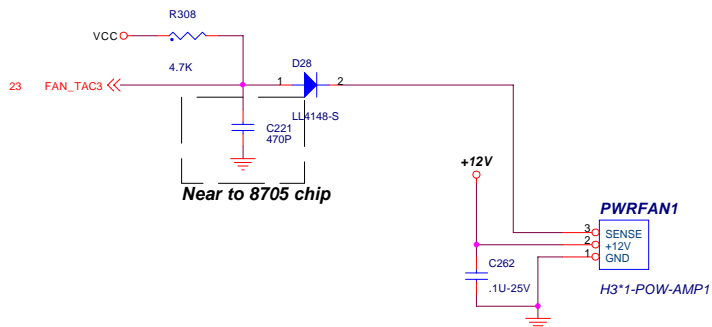
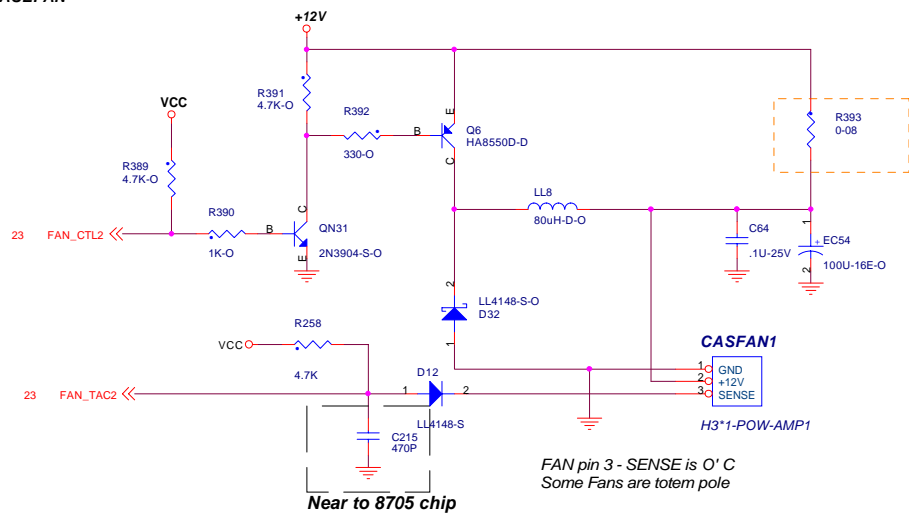
Layout :

Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA

CPUFAN

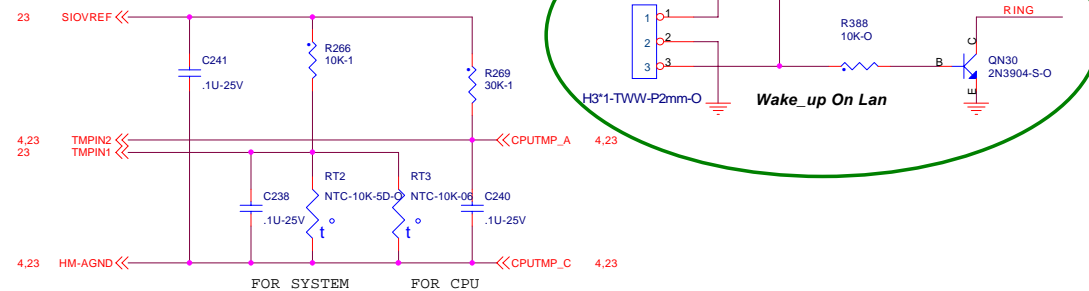


CASEFAN

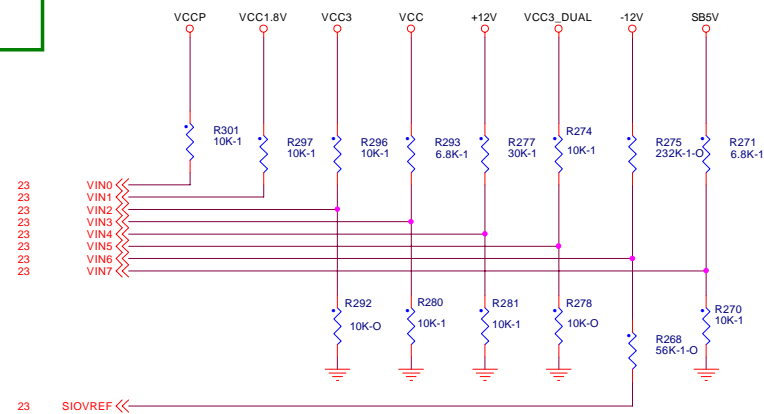


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



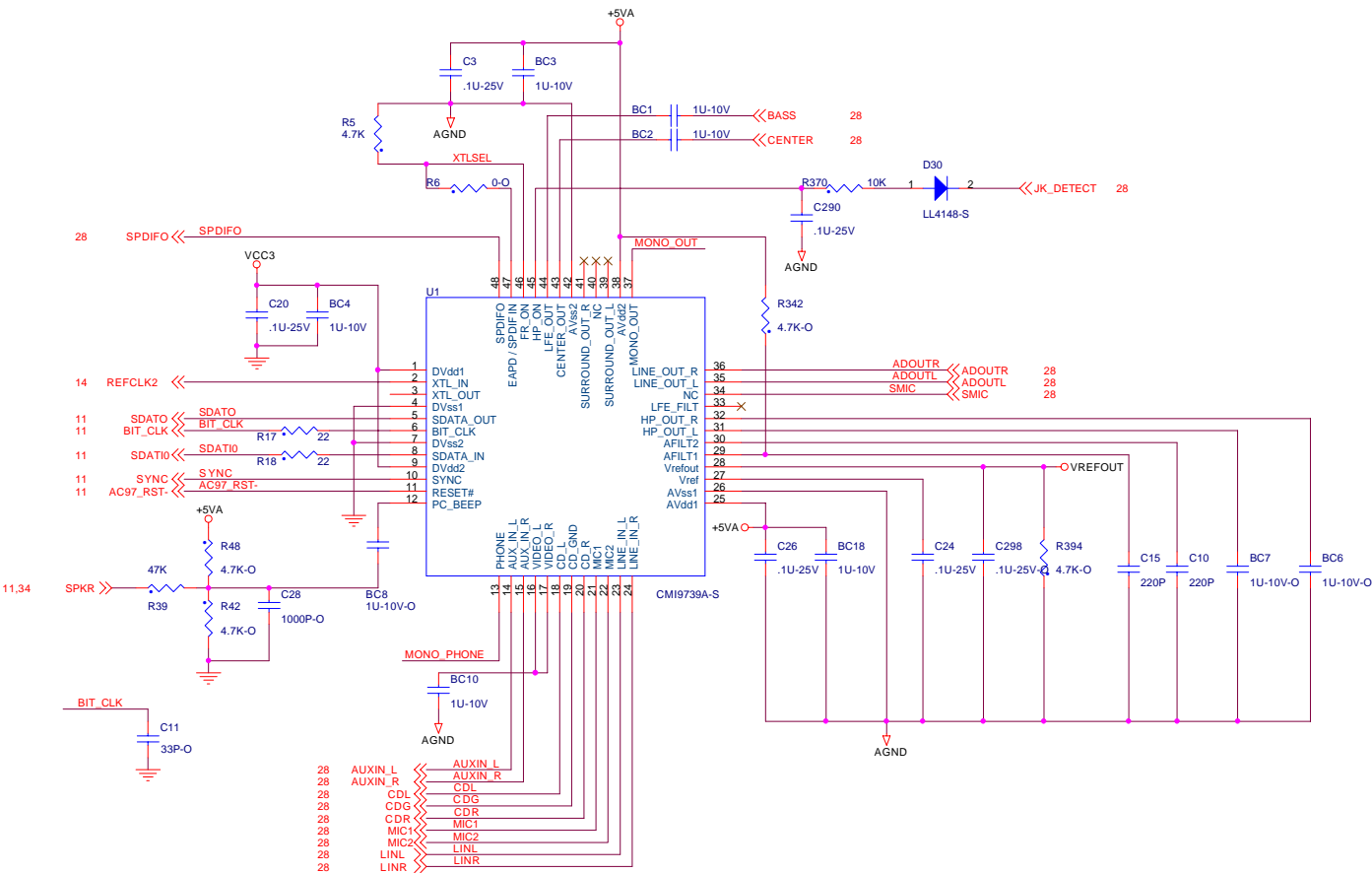
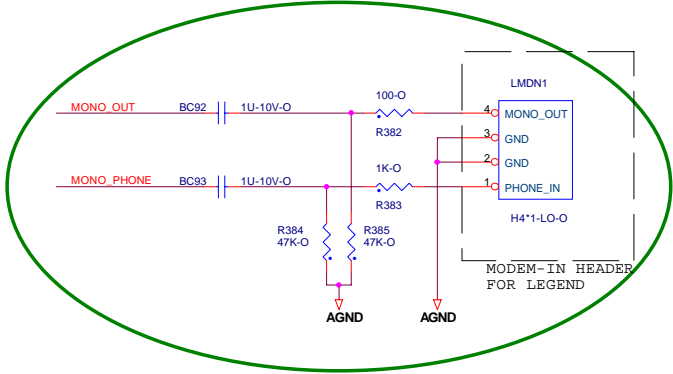
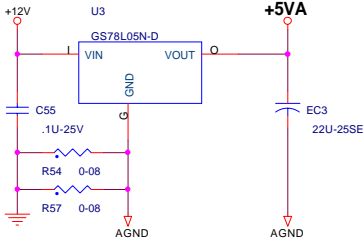
Voltage Monitor



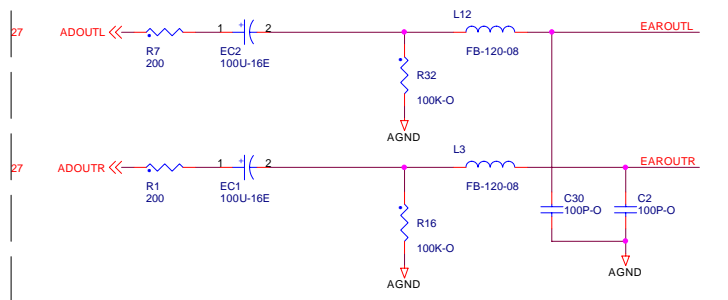
Elitegroup Computer Systems

Title	SF1/648FX		
Size	Document Number	HM / FAN / RING	
Custom			
Date:	Thursday, June 12, 2003	Sheet	26 of 34

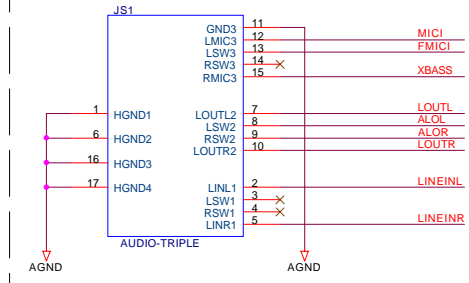
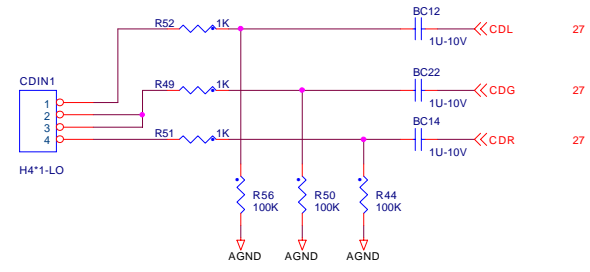
	R14	R6	R5	R4	R342	R2	BC9	BC5	R26	BC9	BC20	R27	L2	BC6	BC7
CMI9738	Open	Open	Open	Open	Open	0	Open	Open	Open	Open	Open	Open	Open	Open	Open
CMI9739A	0	Open	4.7K	Open	Open	Open	Open	Open	Open	Open	1U	3K	FB	Open	Open
CMI9760	0	0	4.7K	Open	4.7K	Open	Open	1U	3K	Open	1U	3K	FB	Open	Open
ALC650-E	0	Open	4.7K	Open	Open	Open	1U	Open	3K	1U	Open	3K	FB	1U	1U



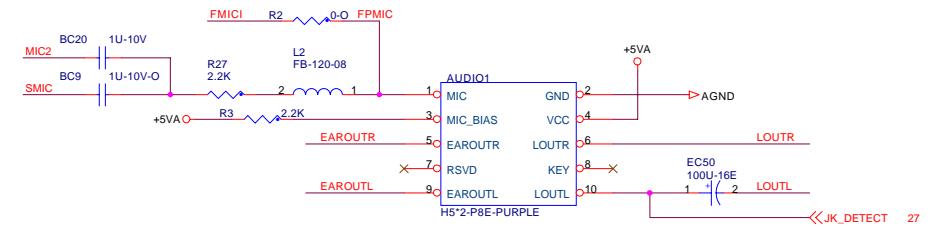
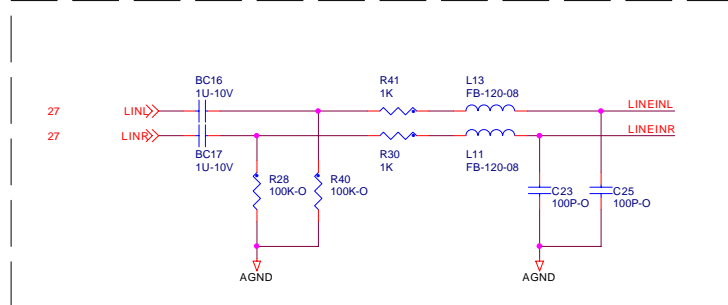
SPEAKER-OUT



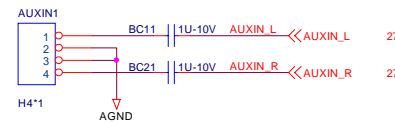
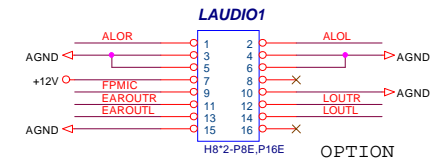
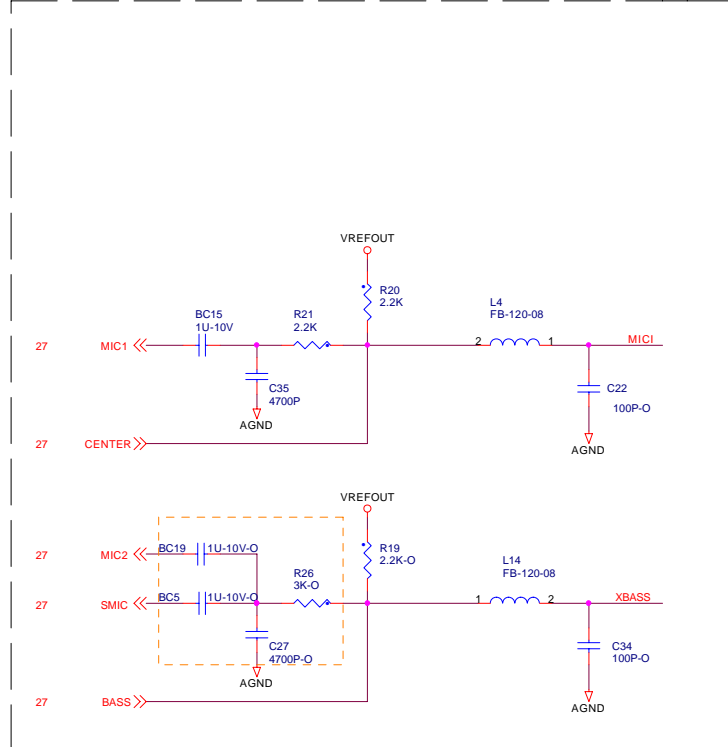
CD-IN



LINE-IN / SURROUND-OUT

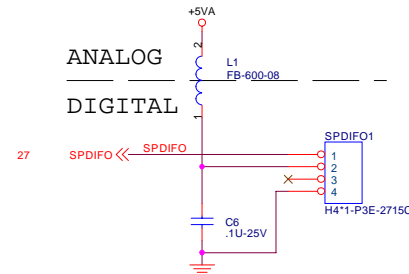


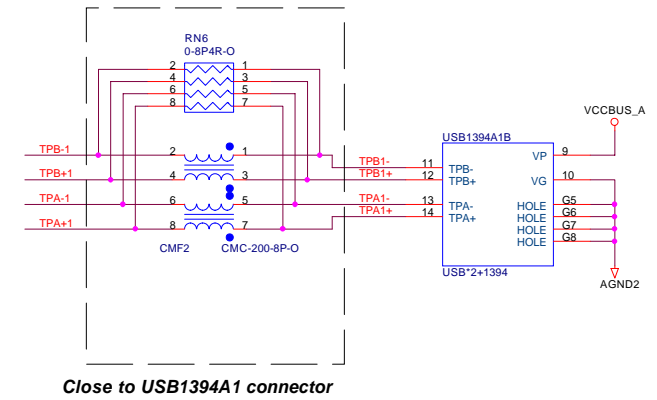
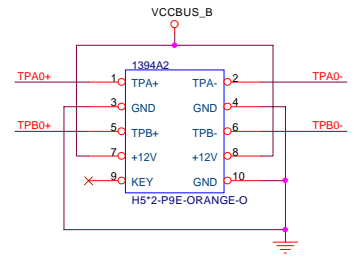
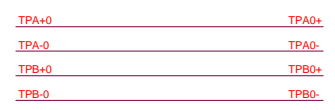
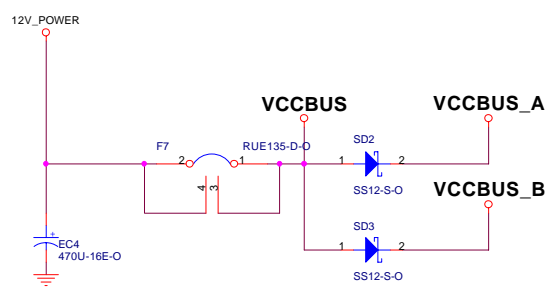
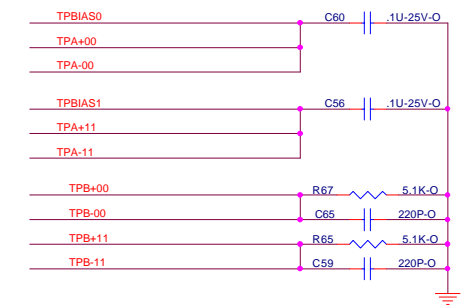
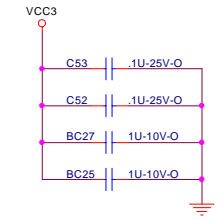
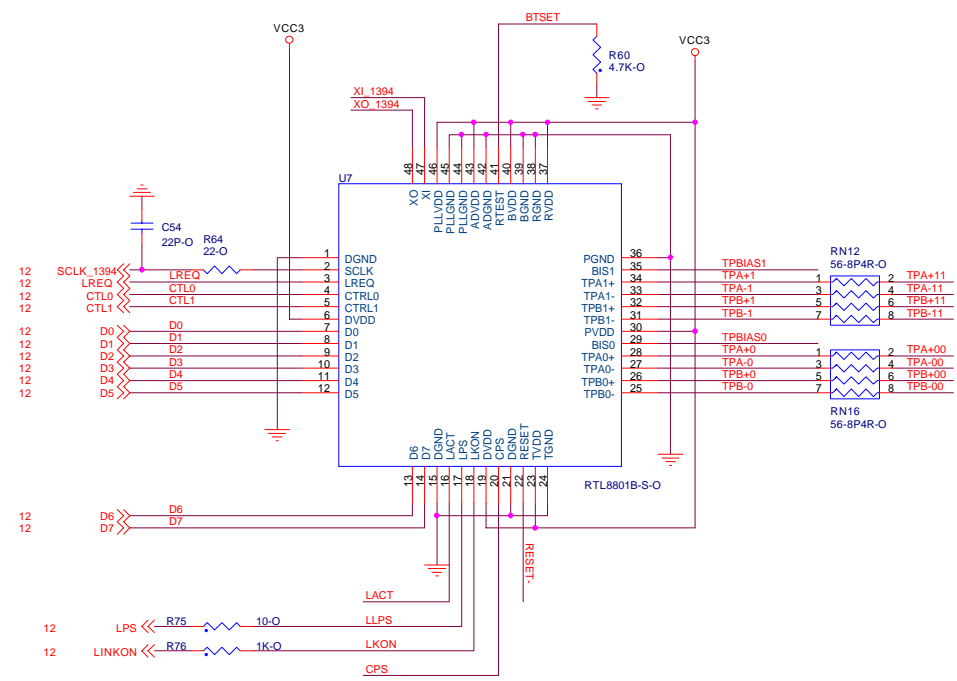
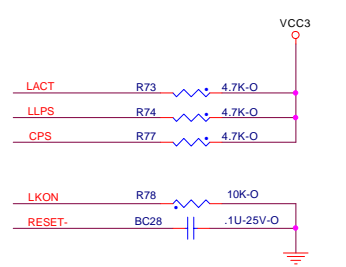
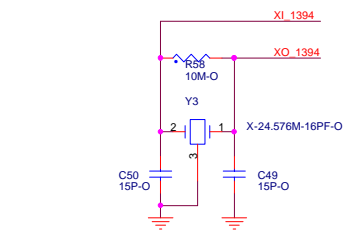
MIC-IN / CENTER-BASS OUT

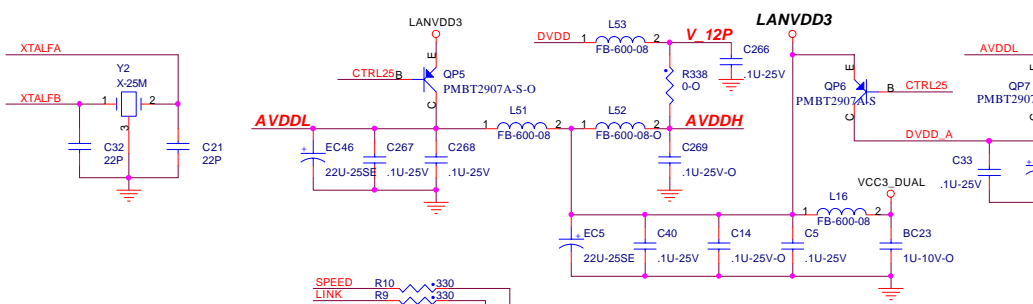


ANALOG

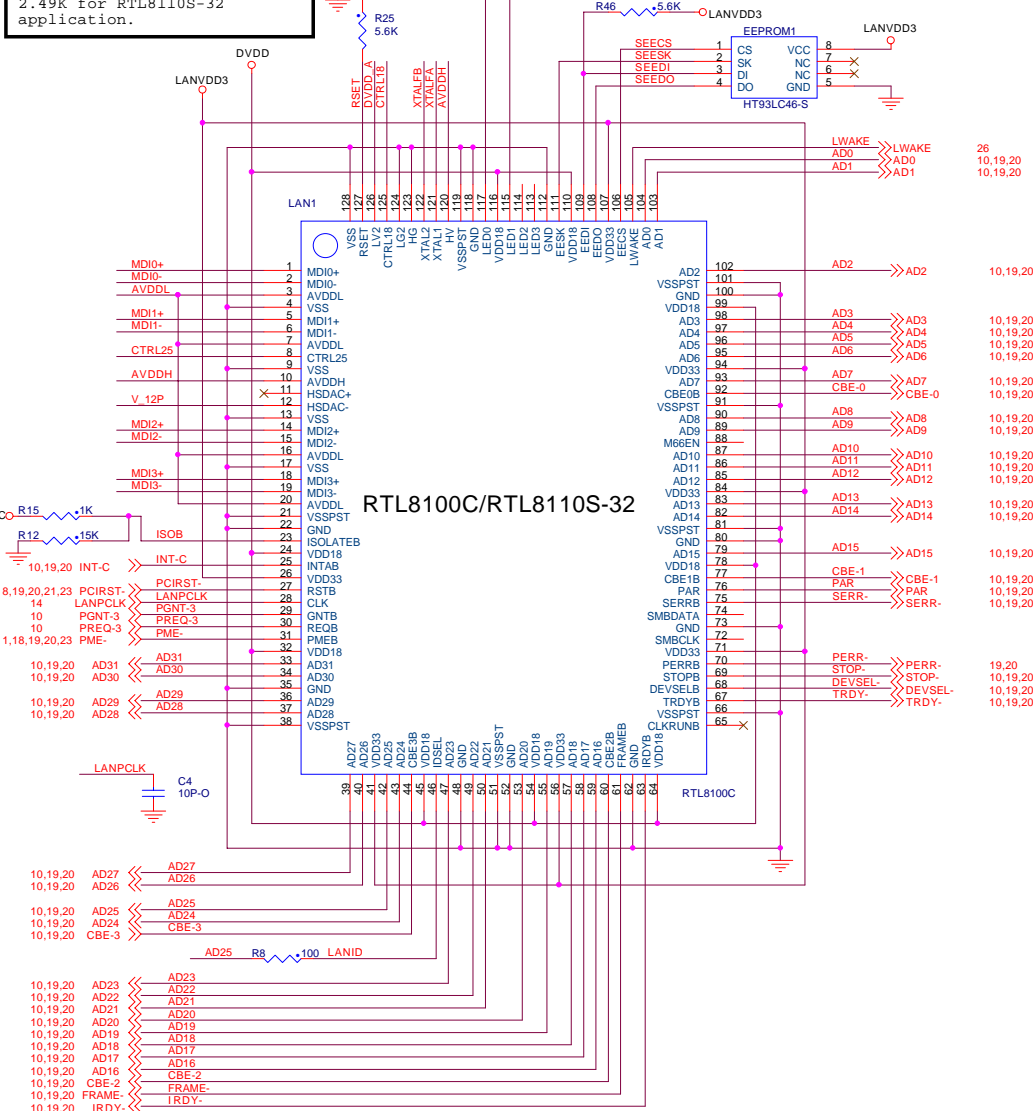
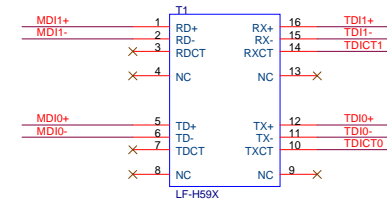
DIGITAL



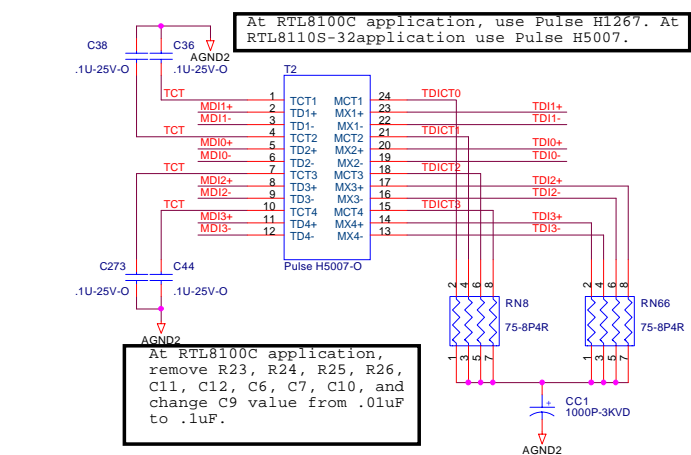




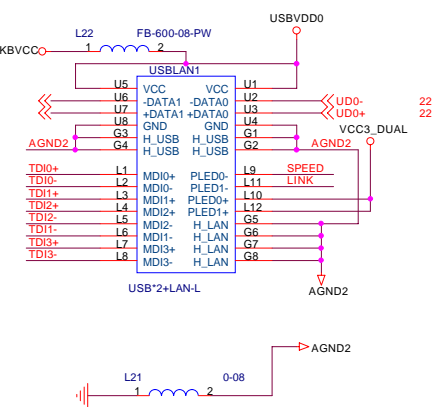
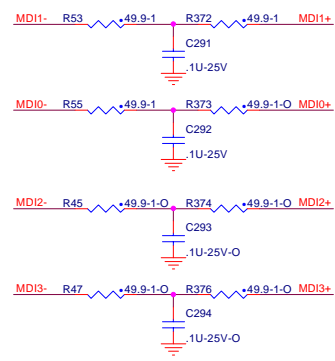
R25 value should be 5.6K at RTL8100C application, and use 2.49K for RTL8110S-32 application.



At RTL8100C application, use Pulse H1267. At RTL8110S-32 application use Pulse H5007.



At RTL8100C application, remove R23, R24, R25, R26, C11, C12, C6, C7, C10, and change C9 value from .01uF to .1uF.



	8100C	8110S
VDD3	3.3V	3.3V
AVDDH	X	3.3V
AVDDL	3.3V	2.5V
DVDD	2.5V	1.8V
DVDD_A	2.5V	1.8V
V_12P	2.5V	X

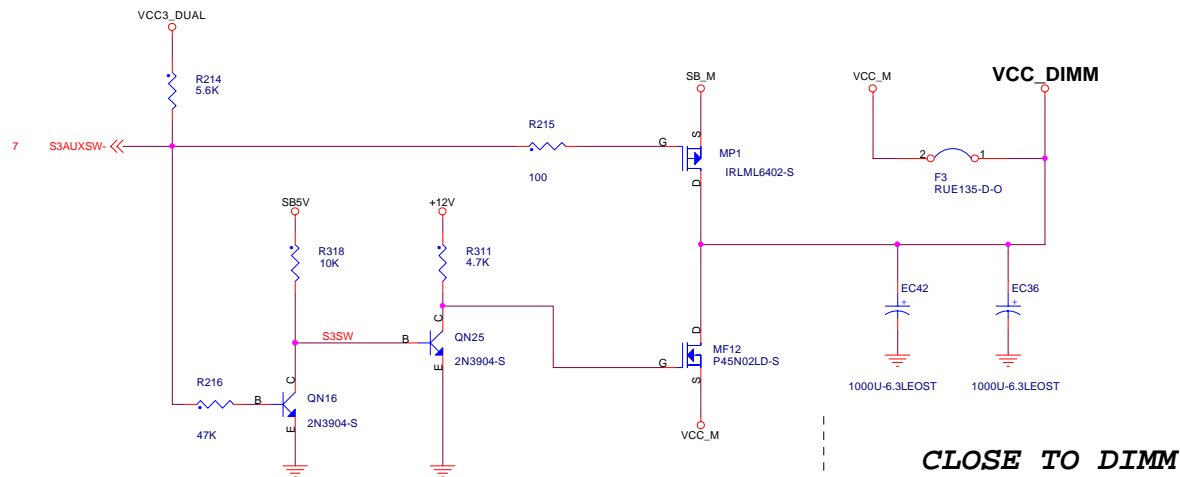
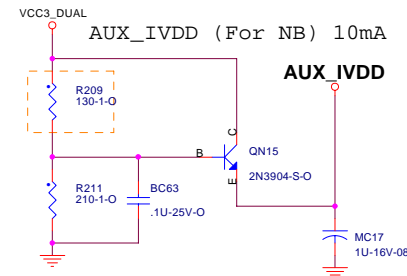
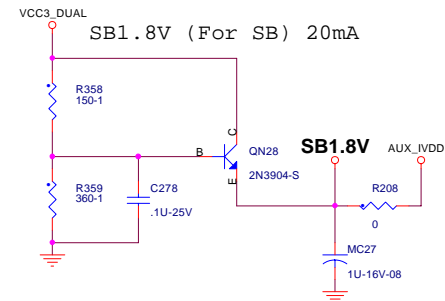
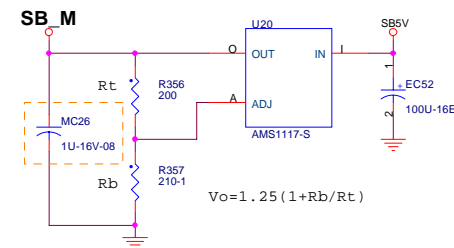
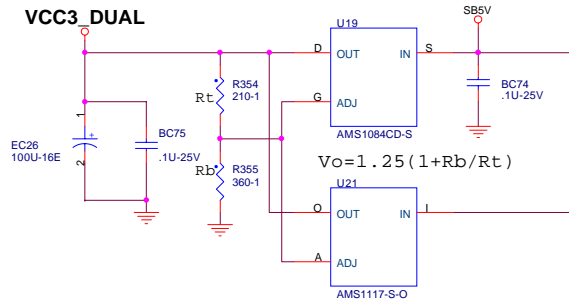
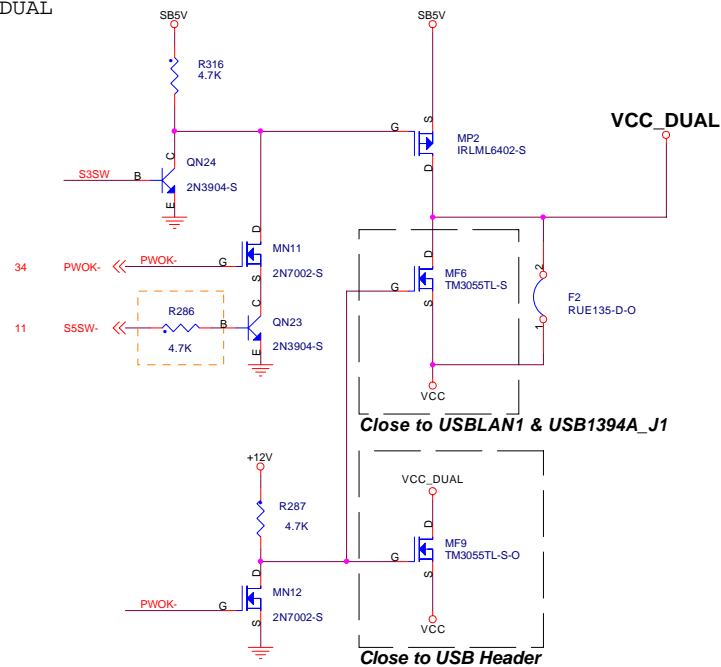
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

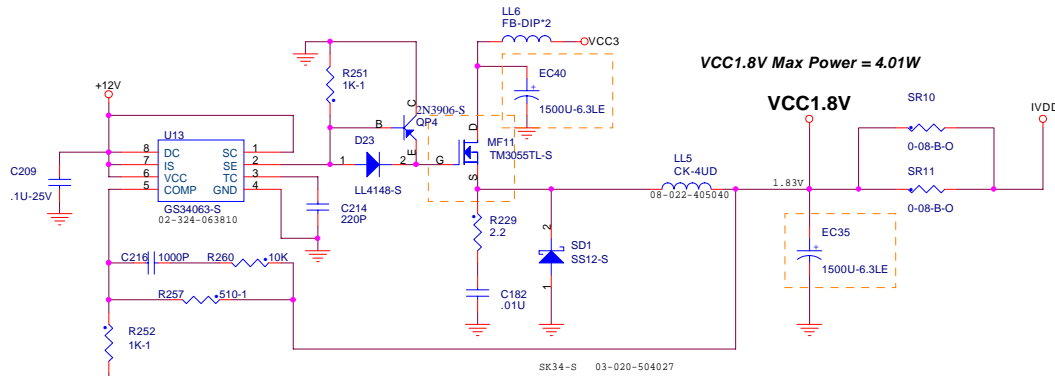
NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER.(ADDITIONAL
500mA PER USB PORT)

VCC3_DUAL & VCC5_DUAL



litegroup Computer Systems

Title	SF1/648FX		
Size	Document Number	Dual 5V&3V, STR	
Custom			Rev 1.0
Date	Saturday, June 26, 2003	Sheet 31	of 34

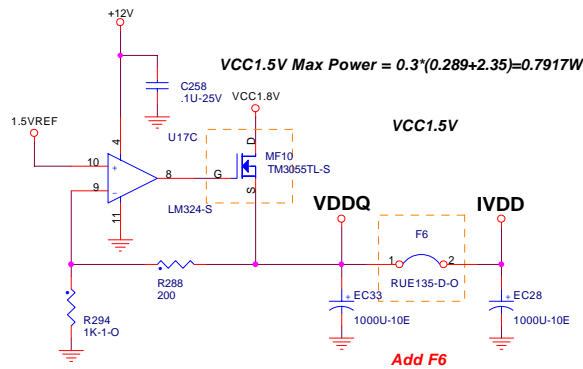


VCC1.8V Max Power = 4.01W

VCC1.8V

	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

	AUX_IVDD	SBI.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator

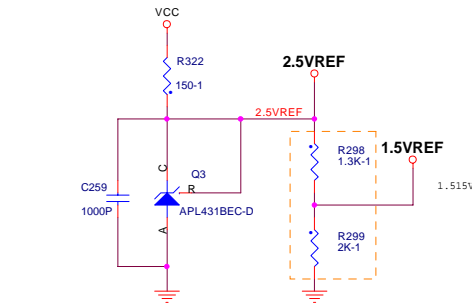


VCC1.5V Max Power = 0.3*(0.289+2.35)=0.7917W

VCC1.5V

F6	
661LV	SHORT
648	OPEN

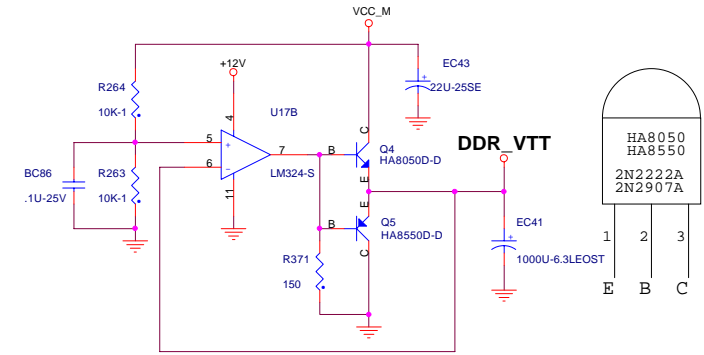
11



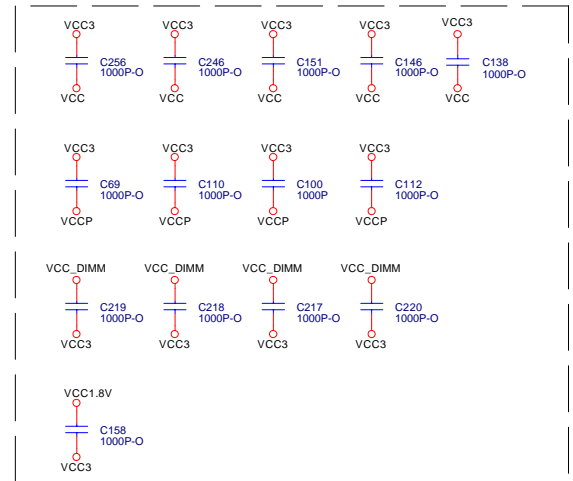
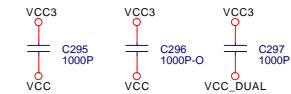
2.5VREF

1.5VREF

DDR_VJ	VCC_M
0	2.54V
1	2.63V

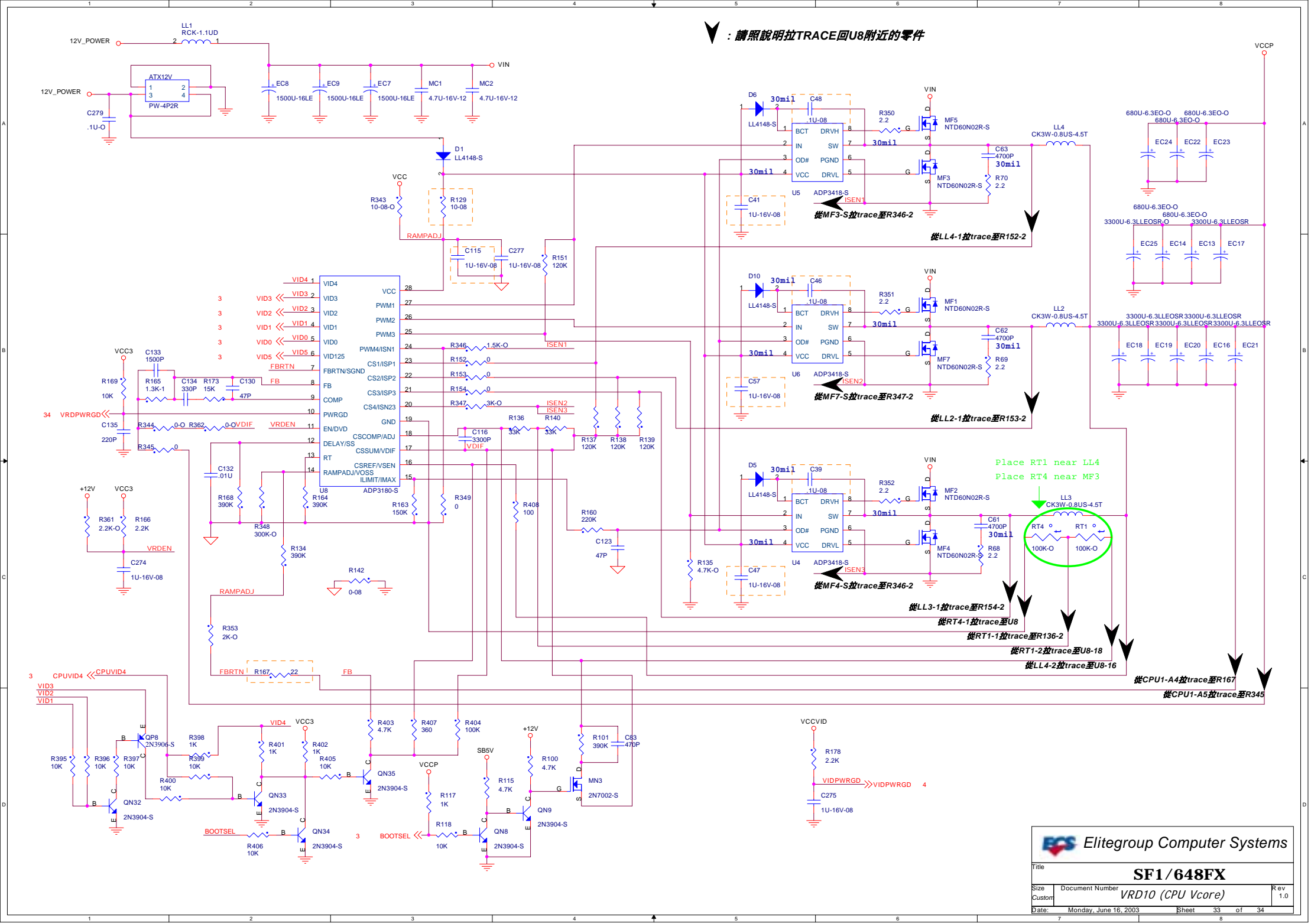


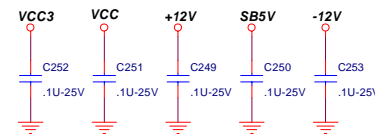
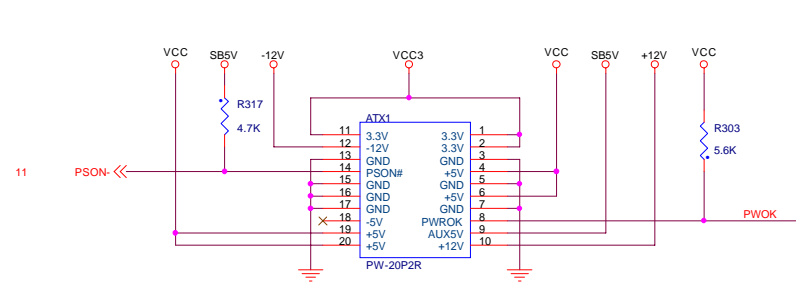
DDR_VTT



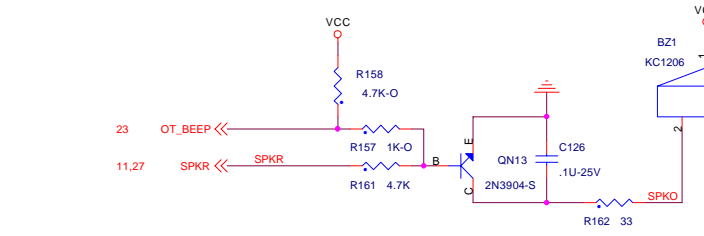
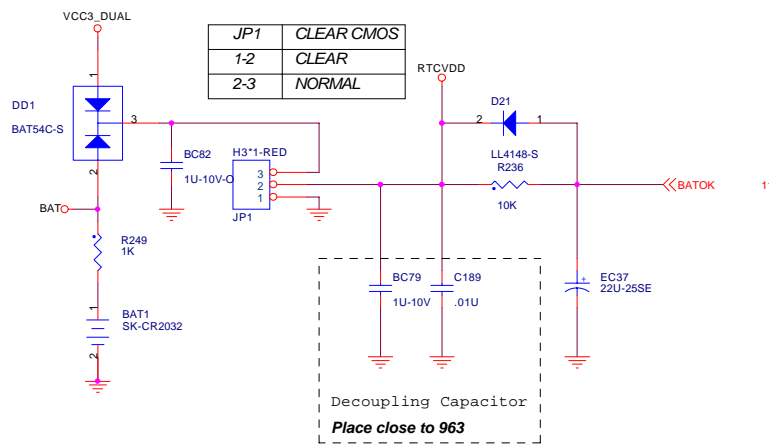
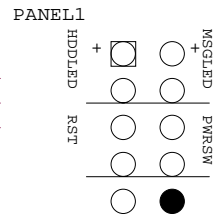
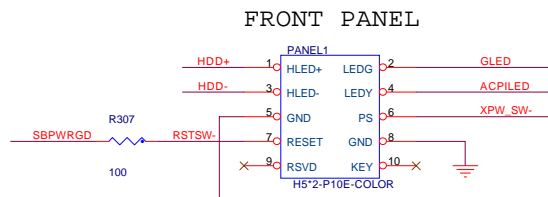
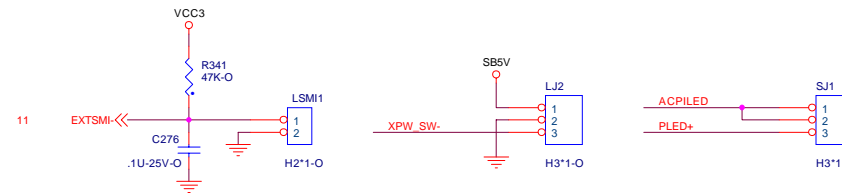
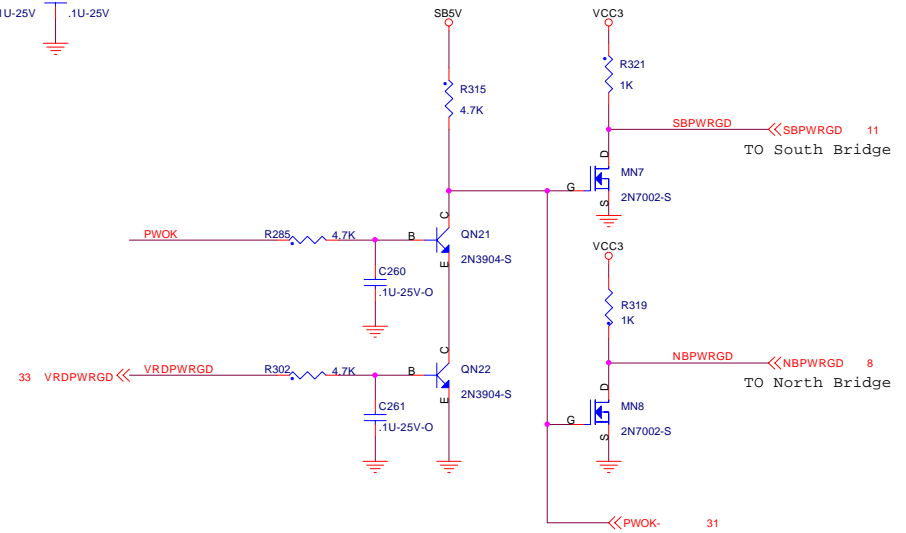
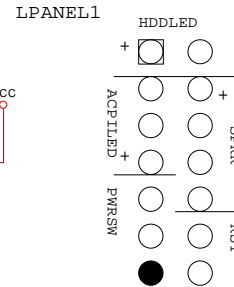
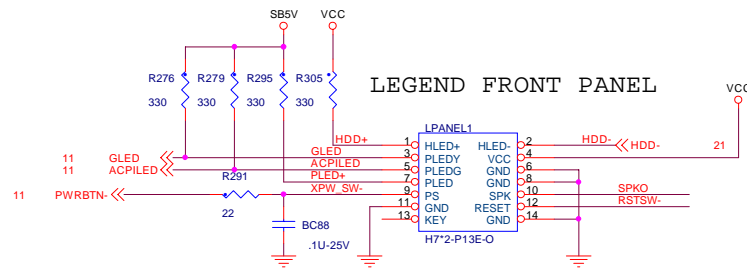
平均分佈在POWER PLAN 和 PLAN 之間

▼ : 請照說明拉TRACE回U8附近的零件





Layout :
Bypass capacitors close to ATX power connector for EMI solution.



RTC

NOTE!
1.The RTCVDD is 3V
2.Decoupling capacitor must be close to 635 RTCVDD pin.
3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.

